



YJT300G10A

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	100V
I_D	300A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	1.55m
$R_{DS(ON)}$ (at $V_{GS}=6V$)	2.4m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Epoxy Meets UL 94 V-0 Flammability Rating



YJT300G10A

Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max
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Typical Electrical and Thermal Characteristics Diagrams

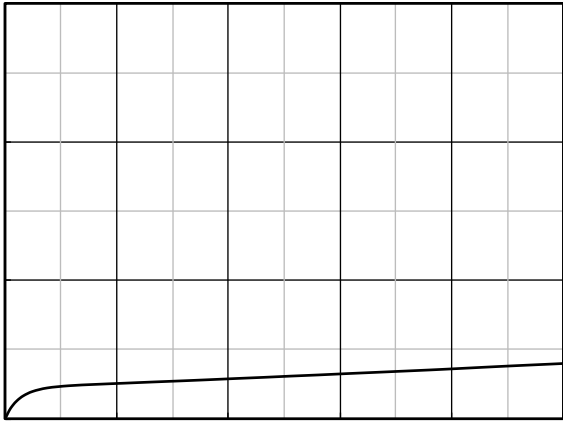


Figure 1. Output Characteristics

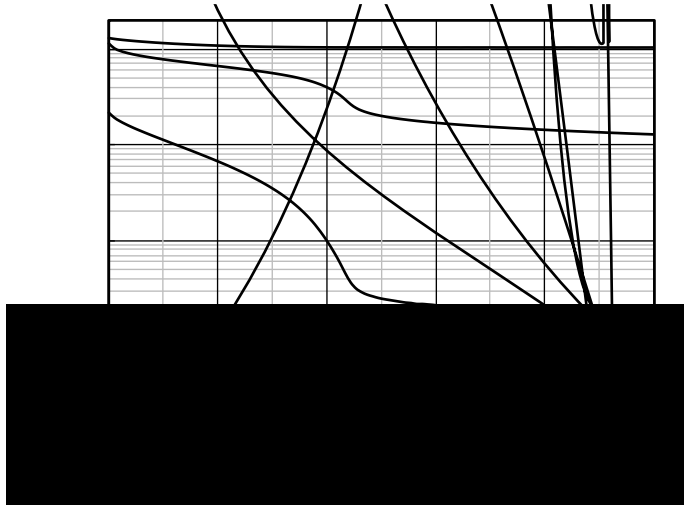


Figure 3. Capacitance Characteristics

Figure 2. Transfer Characteristics

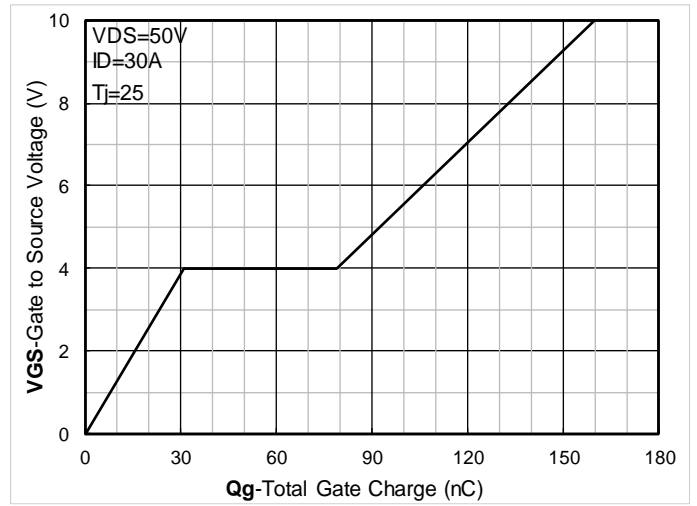


Figure 4. Gate Charge

Figure 5. On-Resistance vs Gate to Source V 0 596.02tag

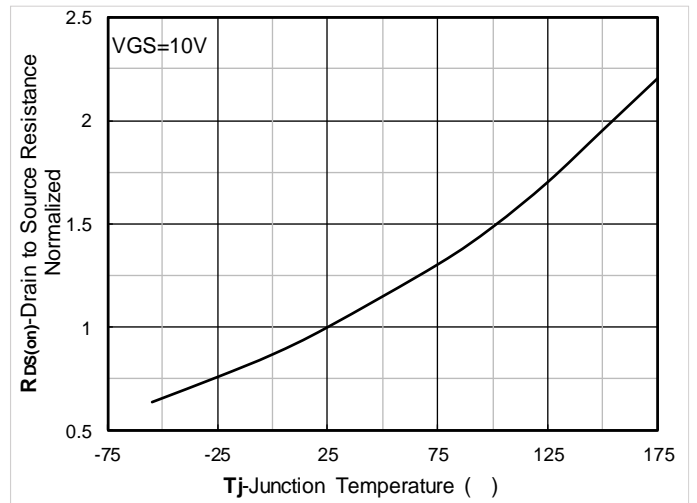


Figure 6. Normalized On-Resistance



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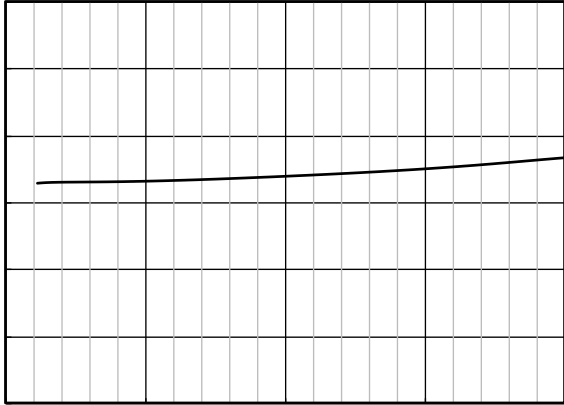


Figure 7. $R_{DS(on)}$ VS Drain Current

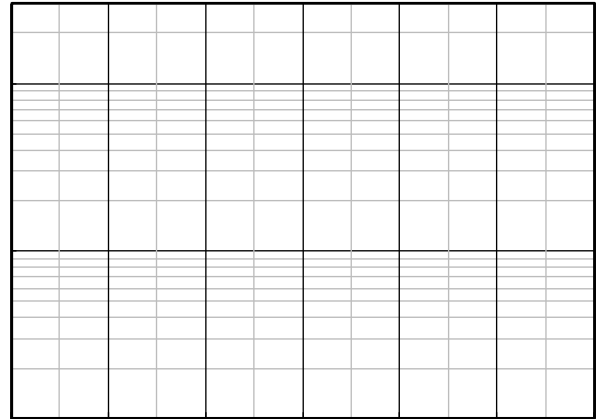


Figure 8. Forward characteristics of reverse diode

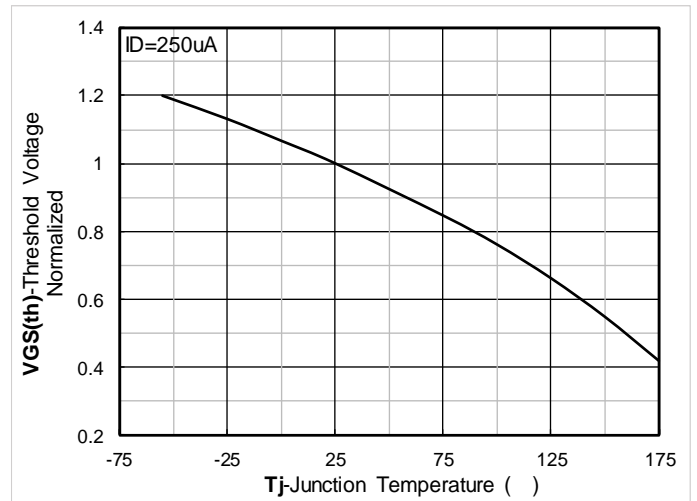


Figure 9. Normalized breakdown voltage

Figure 10. Normalized Threshold voltage

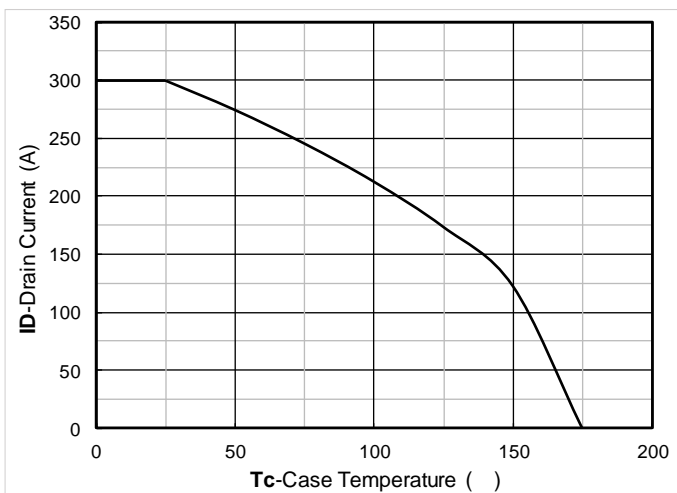


Figure 11. Current dissipation

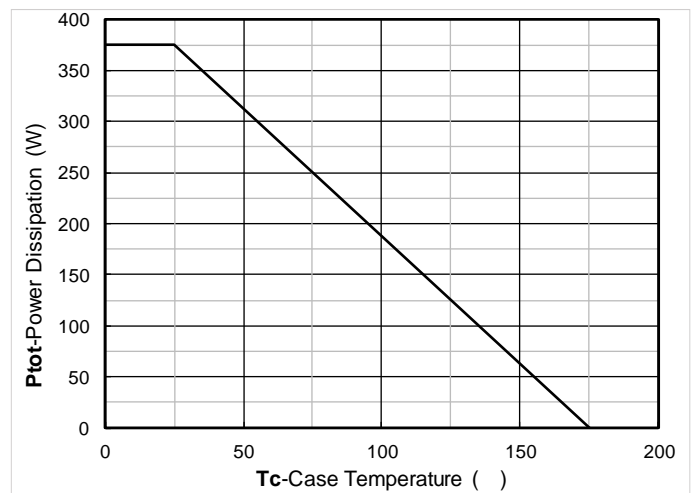


Figure 12. Power dissipation

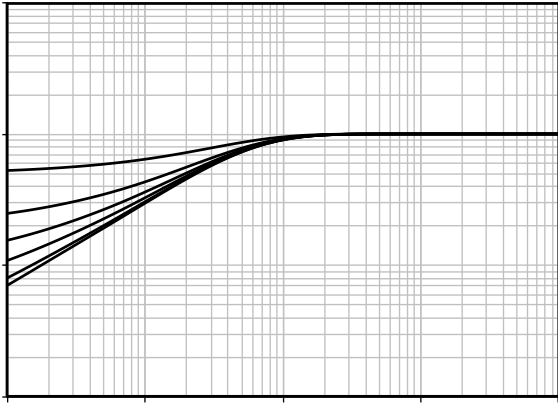


Figure 13. Maximum Transient Thermal Impedance

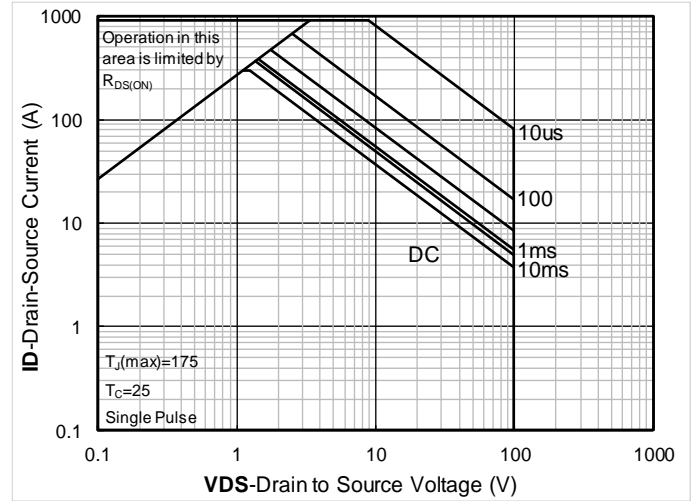


Figure 14. Safe Operation Area

Test Circuits & Waveforms

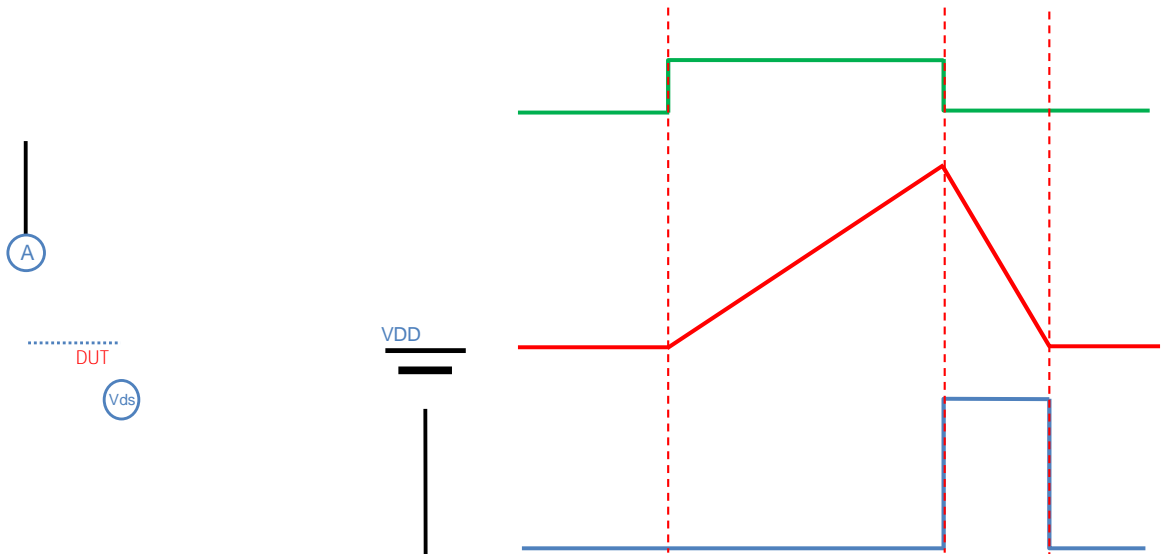


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



Figure B. Gate Charge Test Circuit & Waveform

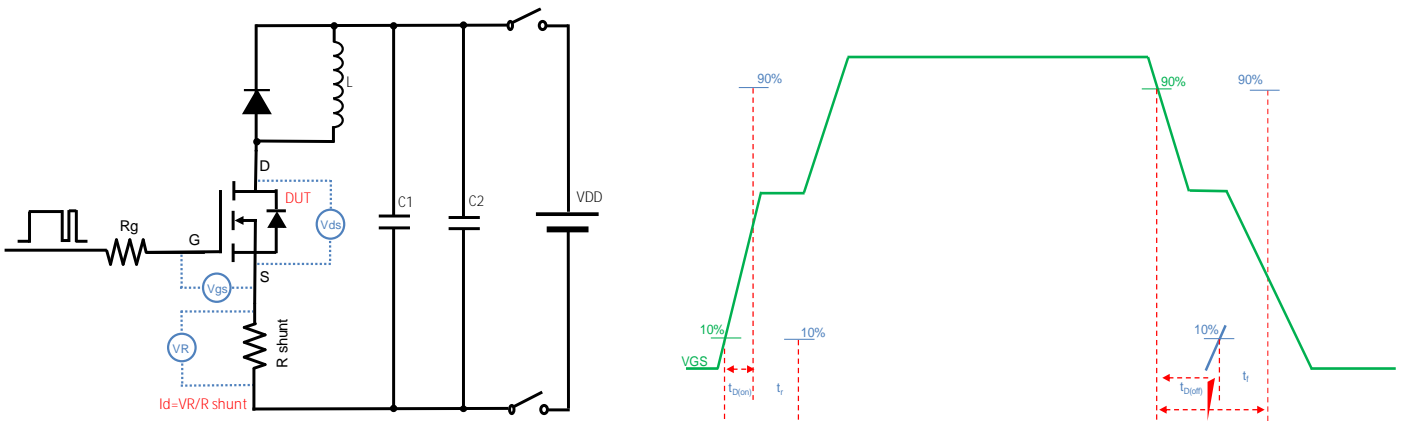


Figure C. Resistive Switching Test Circuit & Waveform

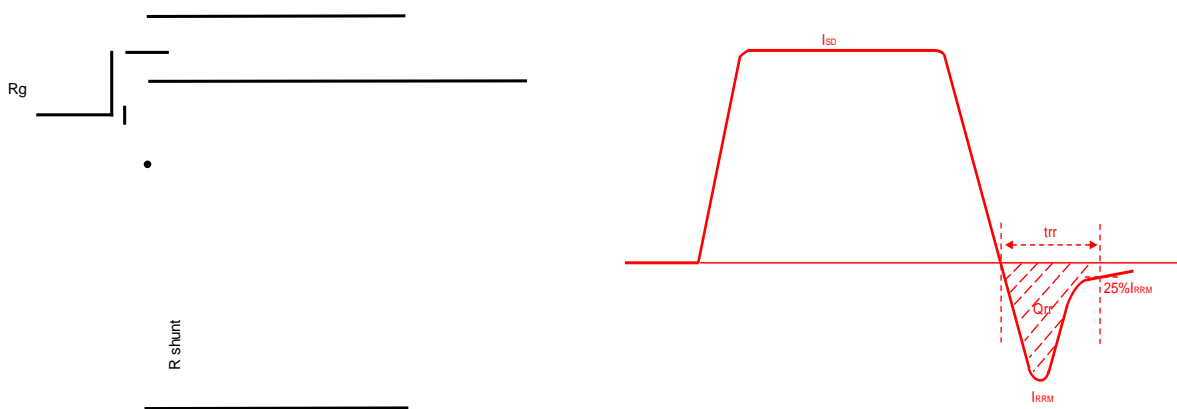


Figure D. Diode Recovery Test Circuit & Waveform



TOLL Package information



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