N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 100V
- I_D 11A
- $R_{DS(ON)}$(at V_{GS}=10V) 13.5mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 17mΩ
- 100% EAS Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen 0.00 EMC 4

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■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	μA
		V_{DS}=100V, V_{GS}=0V, Tj=150	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.7	3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=11A	-	10.5	13.5	mΩ
		V_{GS}=4.5V, I_D=11A	-	13	17	
Diode Forward Voltage	V_{SD}	I_S				

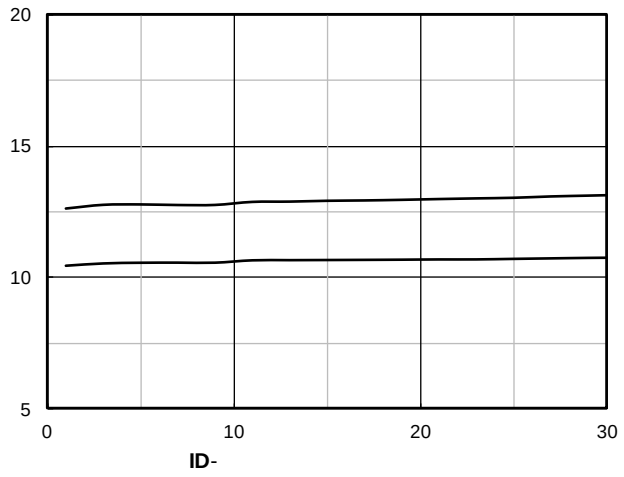

Figure 7. $R_{DS(on)}$ VS Drain Current

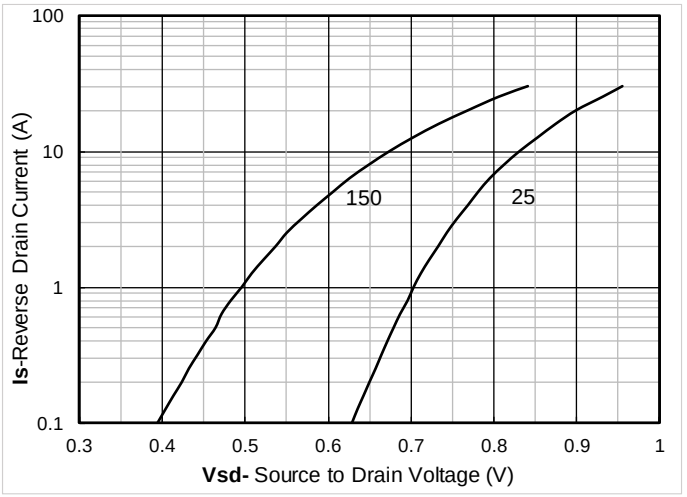

Figure 8. Forward characteristics of reverse diode

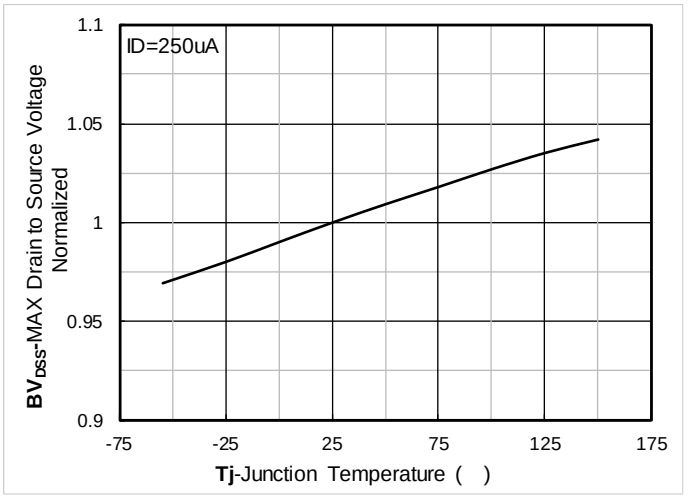

Figure 9. Normalized breakdown voltage

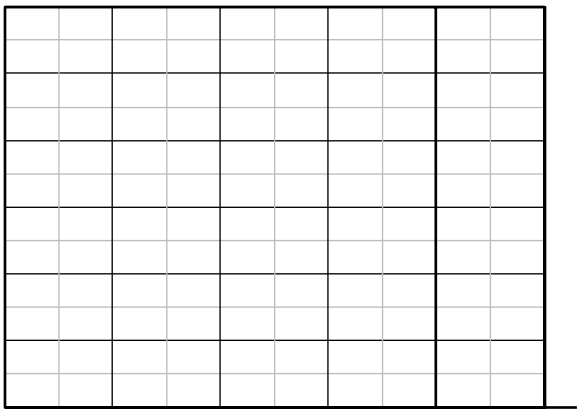

Figure 10. Normalized Threshold voltage

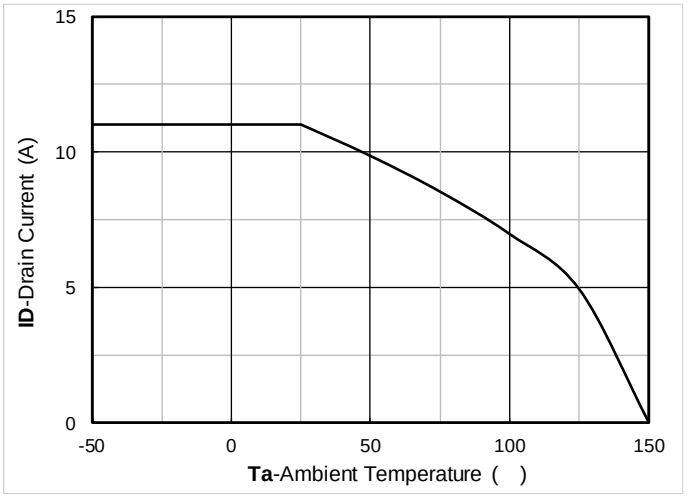

Figure 11. Current dissipation

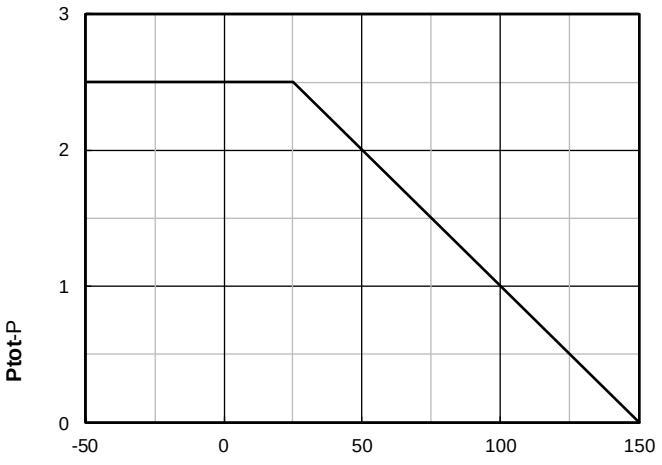

Figure 12. Power dissipation

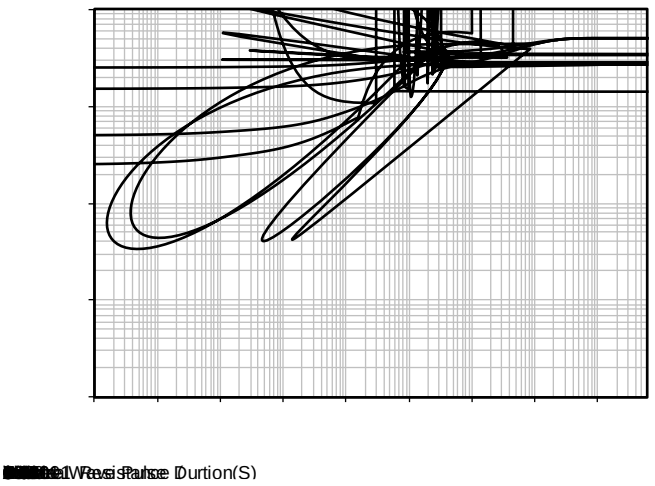

Figure 13. Maximum Transient Thermal Impedance

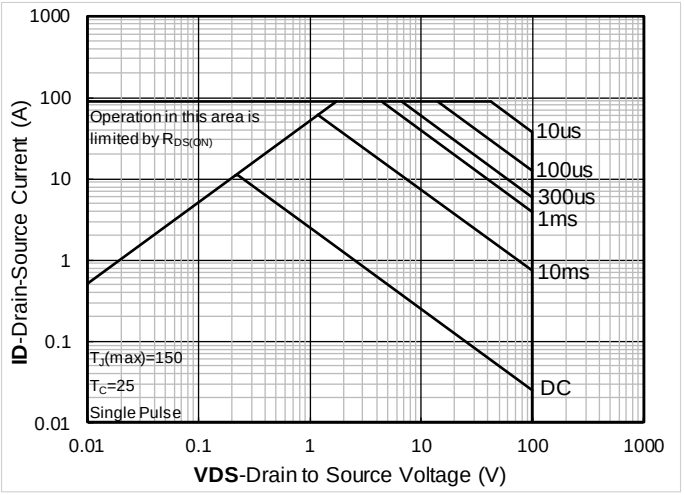

Figure 14. Safe Operation Area

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