# N-Channel Enhancement Mode Field Effect Transistor

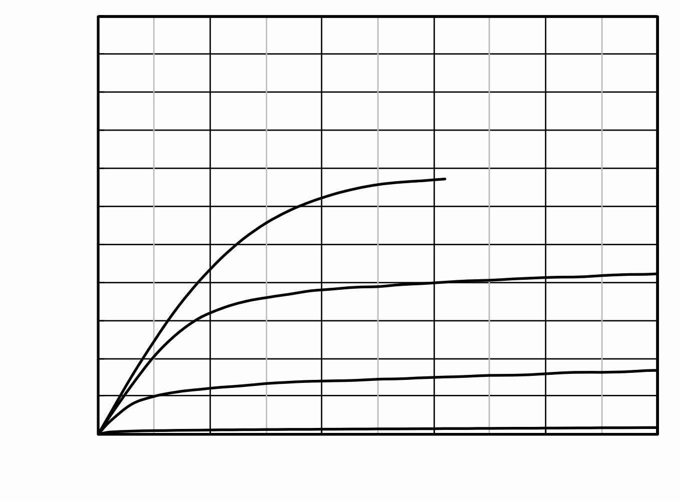
## Product Summary

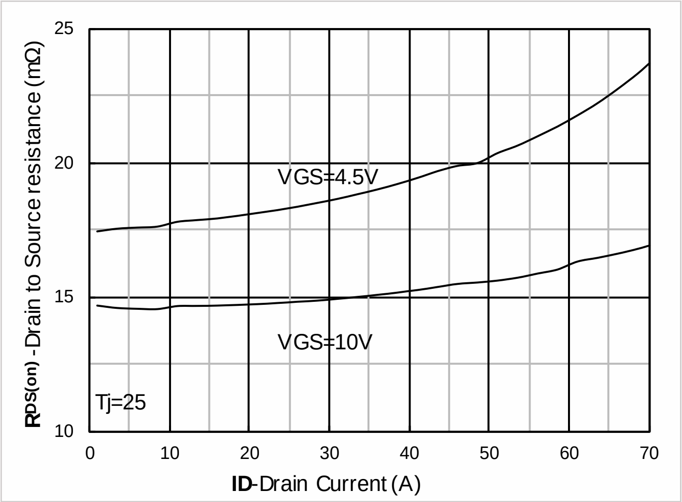
| | |
|---|---|
| ● $V_{DS}$ | 100V |
| ● $I_D$ | 40A |
| ● $R_{DS(ON)}$( at $V_{GS}$ | |

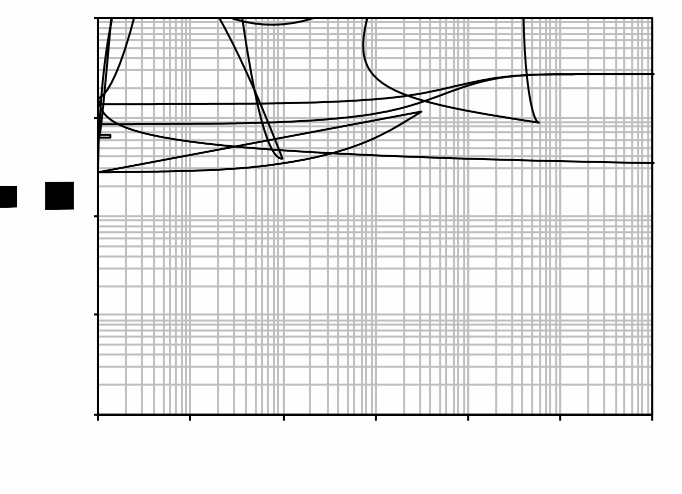
■ **Electrical Characteristics** ($T_J$=25 unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max |
|---|---|---|---|---|---|

## ■Typical Electrical and Thermal Characteristics Diagrams




RDS(on) -Drain to Source resistance (mΩ)
25
20
15
10
VGS=4.5V
VGS=10V
Tj=25
0
10
20
30
40
50
60
70
ID-Drain Current (A)



## ■ Test Circuits & Waveforms

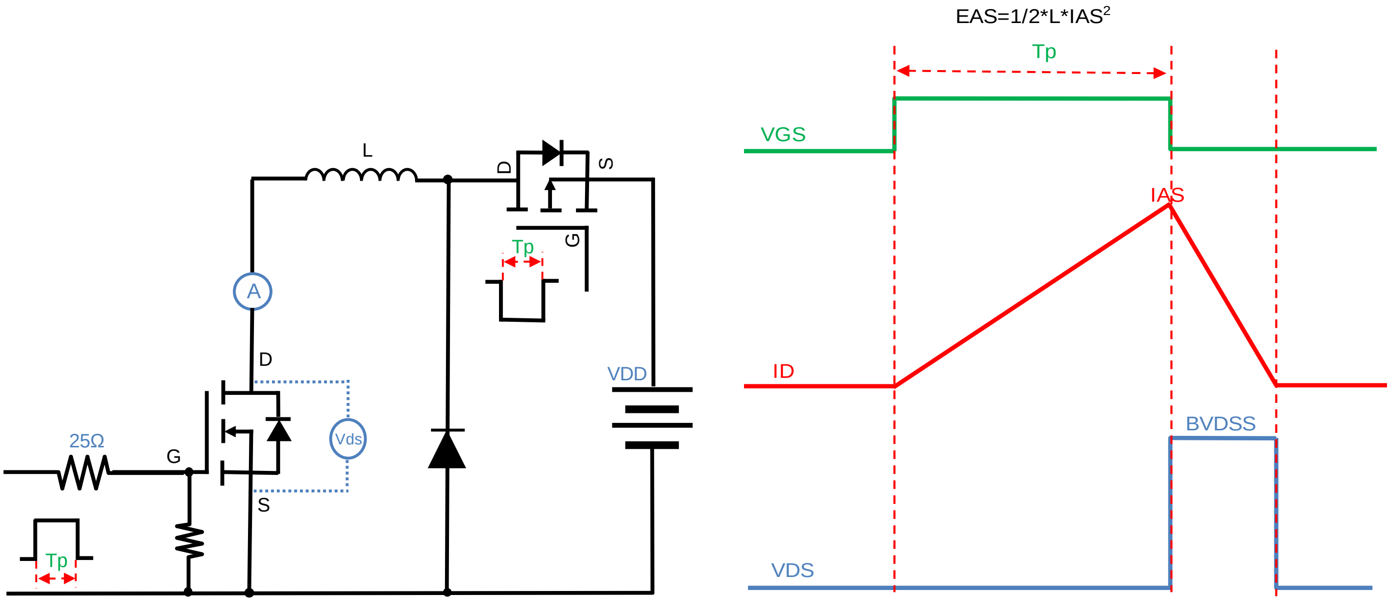
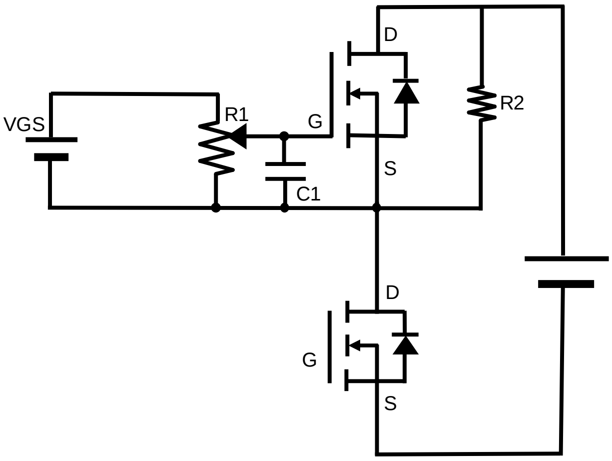
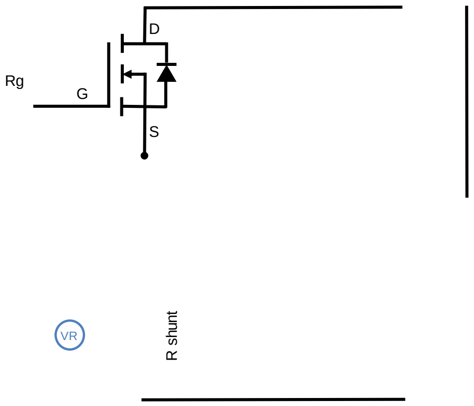
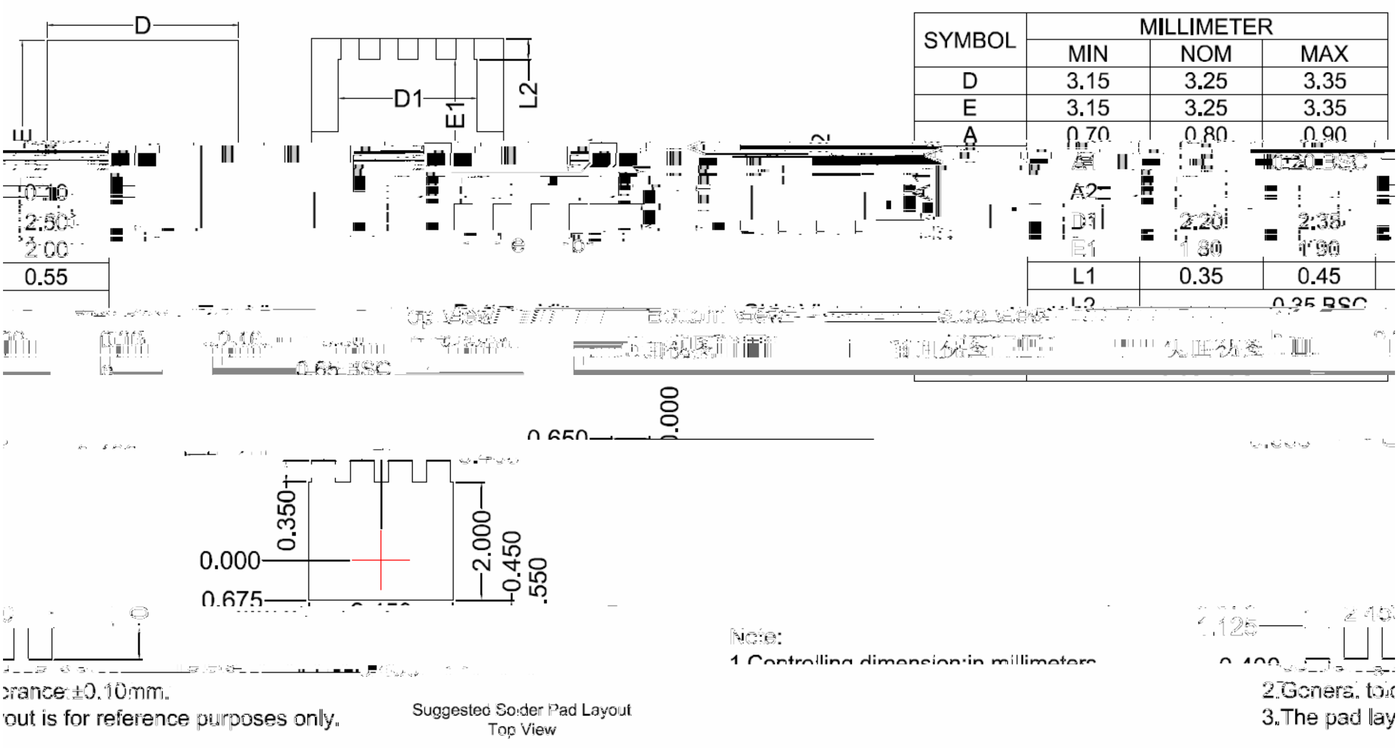


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform




Rg
G
D
S
VR
R shunt

## ■DFN3333-8L Package information



| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| D | 3.15 | 3.25 | 3.35 |
| E | 3.15 | 3.25 | 3.35 |
| A | 0.70 | 0.80 | 0.90 |
| A1 | [illegible] | [illegible] | [illegible] |
| A2 | [illegible] | [illegible] | [illegible] |
| b | 0.20 BSC | | |
| D1 | 2.20 | 2.35 | [illegible] |
| E1 | 1.80 | 1.90 | [illegible] |
| L1 | 0.35 | 0.45 | [illegible] |
| L2 | 0.35 BSC | | |

Suggested Solder Pad Layout
Top View

## Disclaimer

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