N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 30V
- I_D 55A
- $R_{DS(ON)}$(at V_{GS}=10V) 6.5mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 12mΩ
- 100% EAS Tested
- 100% V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
-

Typical Electrical and Thermal Characteristics Di agrams

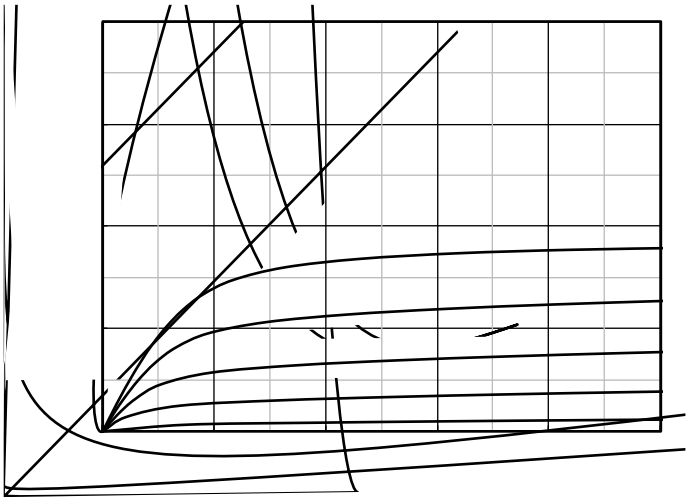


Figure 1. Output Characteristics

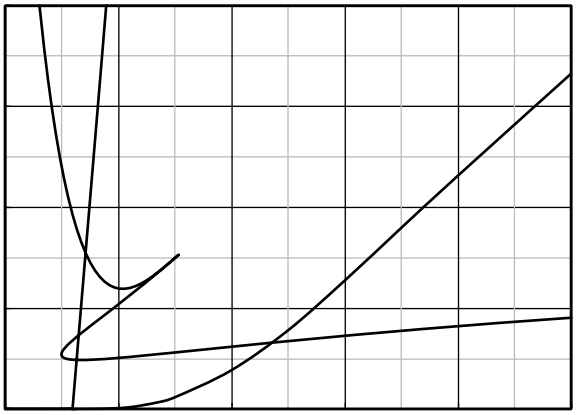


Figure 2. Transfer Characteristics

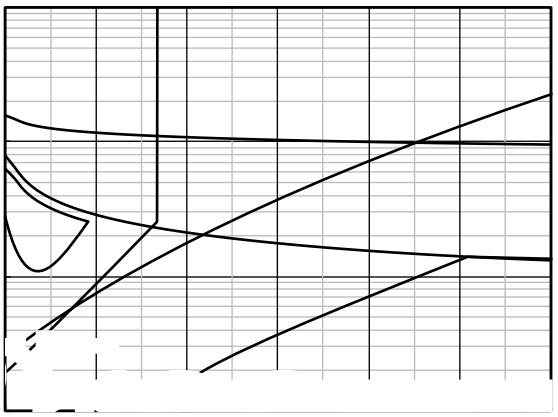


Figure 3. Capacitance Characteristics

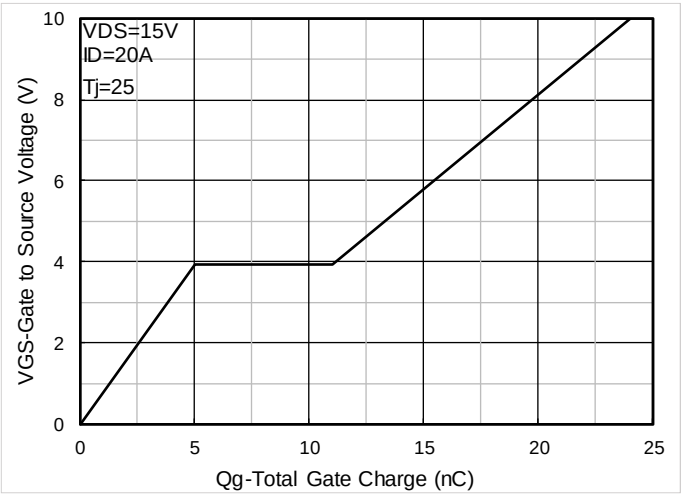


Figure 4. Gate Charge

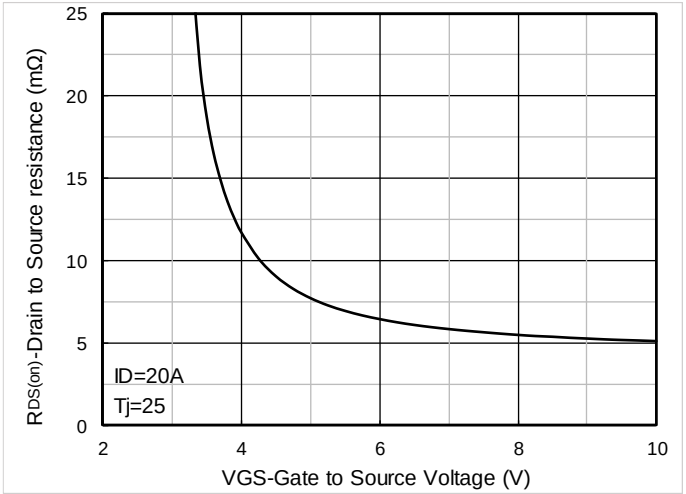


Figure 5. On-Resistance vs Gate to Source Voltage

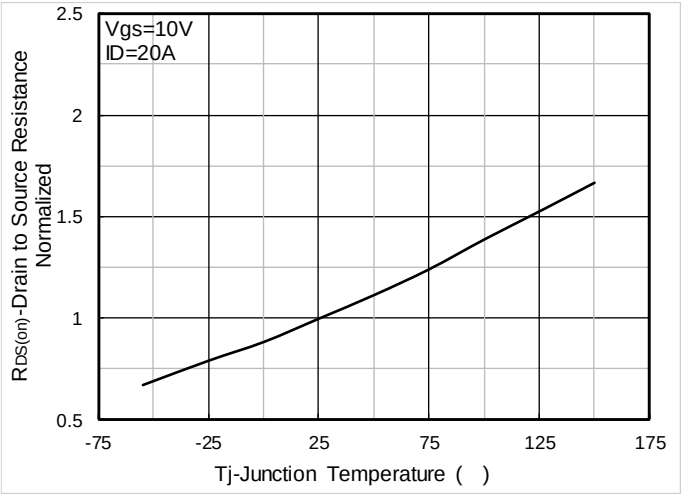
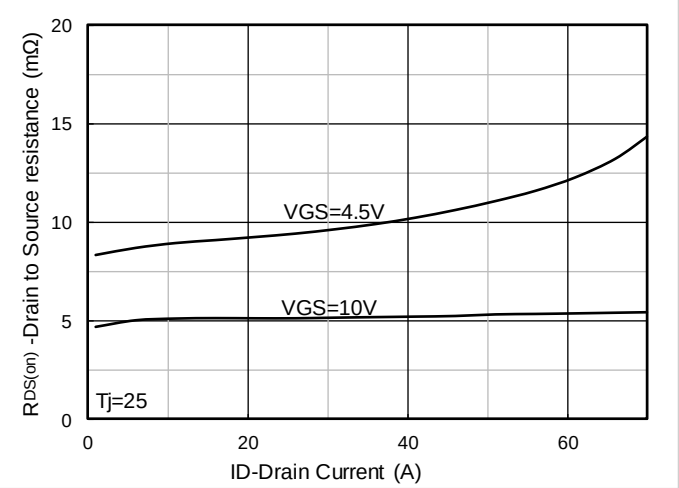


Figure 6. Normalized On-Resistance


20
15
10
5
0
RDS(on) -Drain to Source resistance (mΩ)
VGS=4.5V
VGS=10V
Tj=25
0
20
40
60
ID-Drain Current (A)

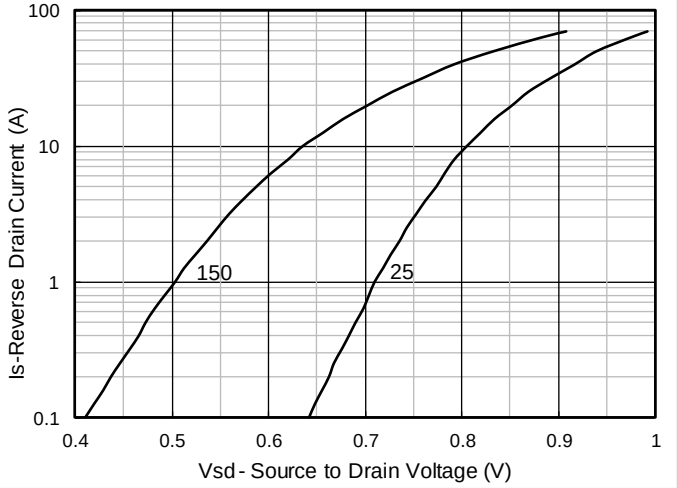

100
10
1
0.1
Is-Reverse Drain Current (A)
150
25
0.4
0.5
0.6
0.7
0.8
0.9
1
Vsd - Source to Drain Voltage (V)

Figure 7. RDS(

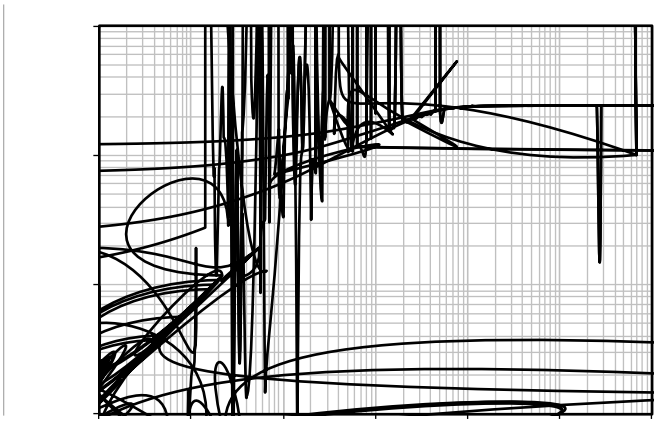


Figure 13. Maximum Transient Thermal Impedance

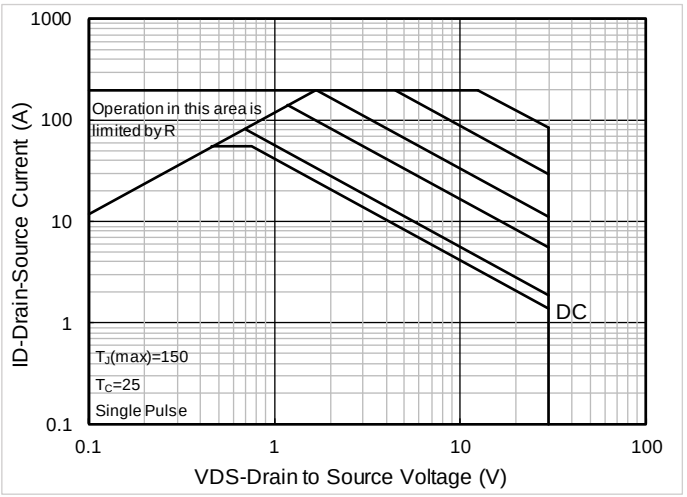


Figure 14. Safe Operation Area

■ Test Circuit s & Waveforms

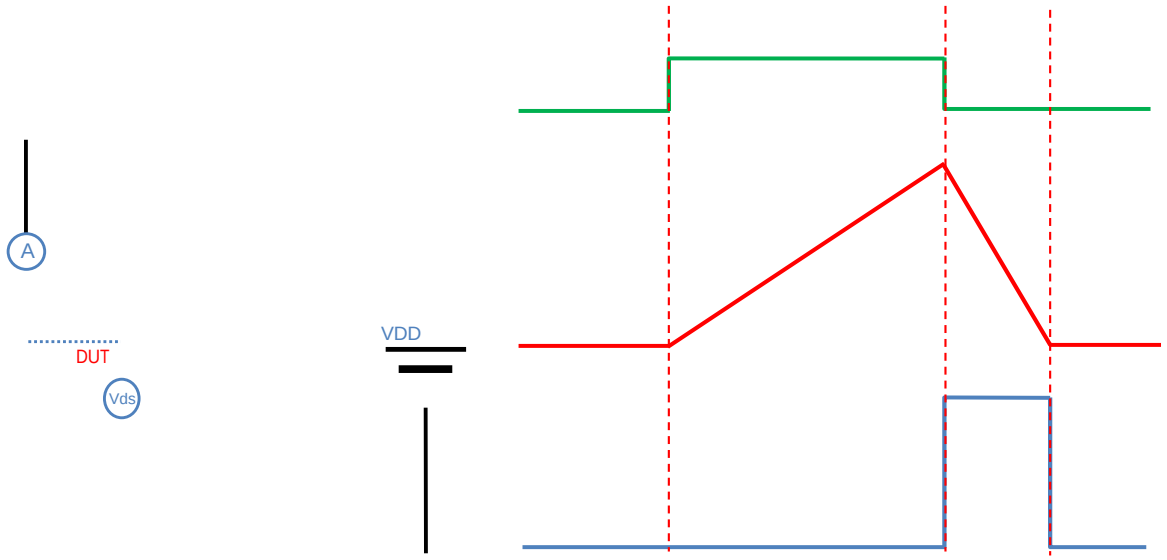


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

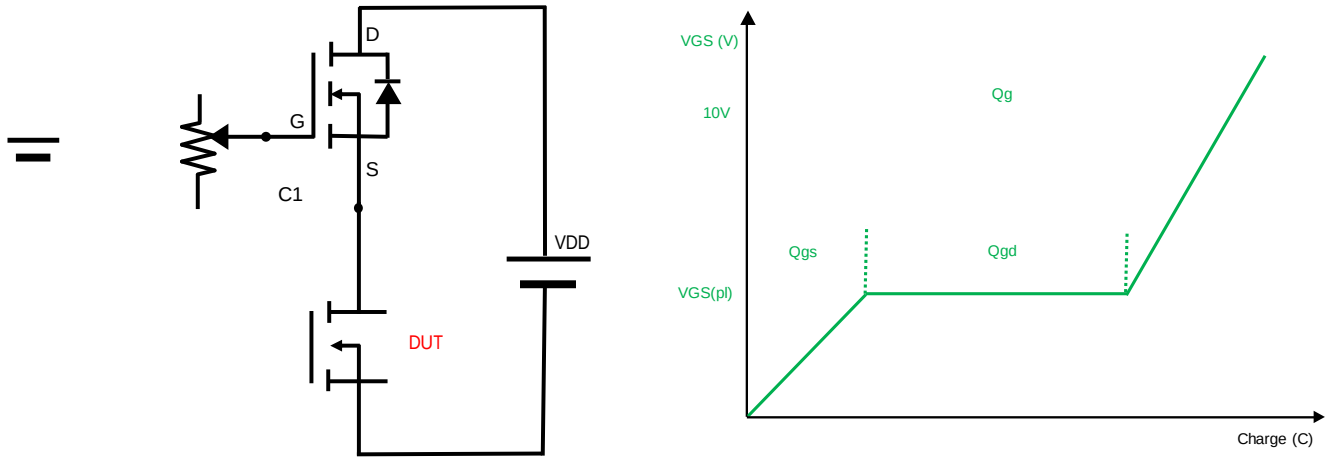


Figure B. Gate Charge Test Circuit & Waveform

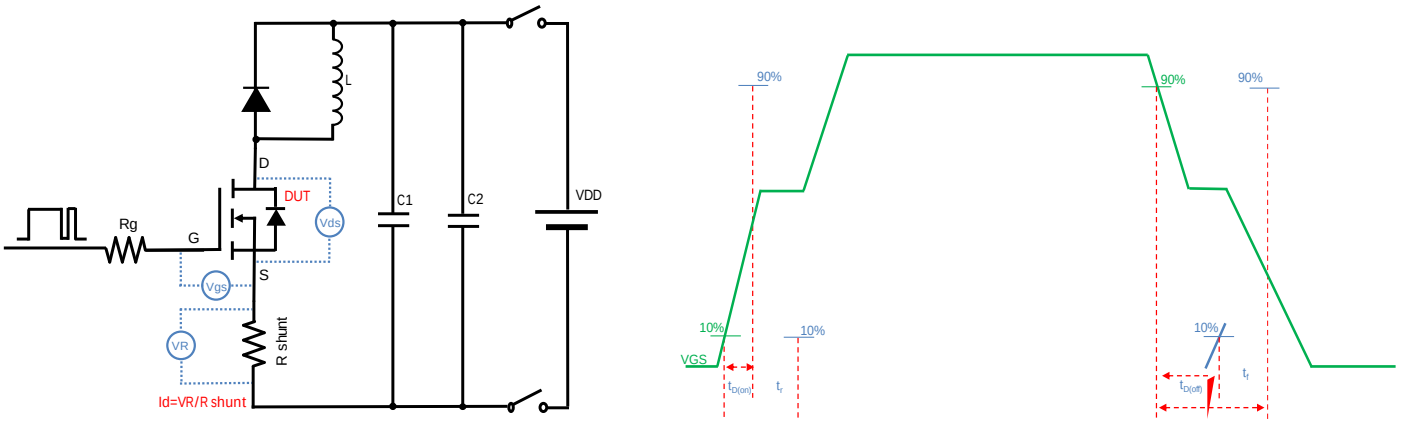


Figure C. Resistive Switching Test Circuit & Waveform

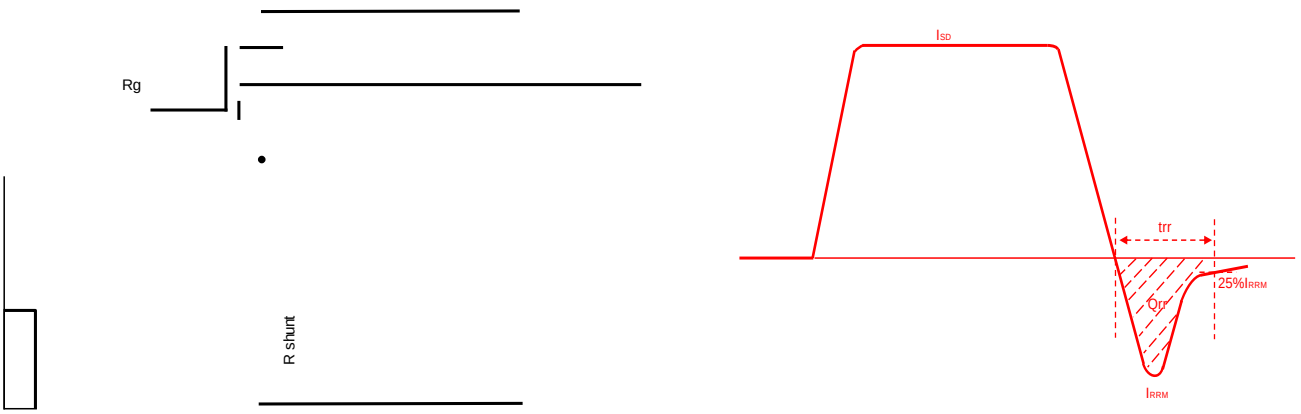
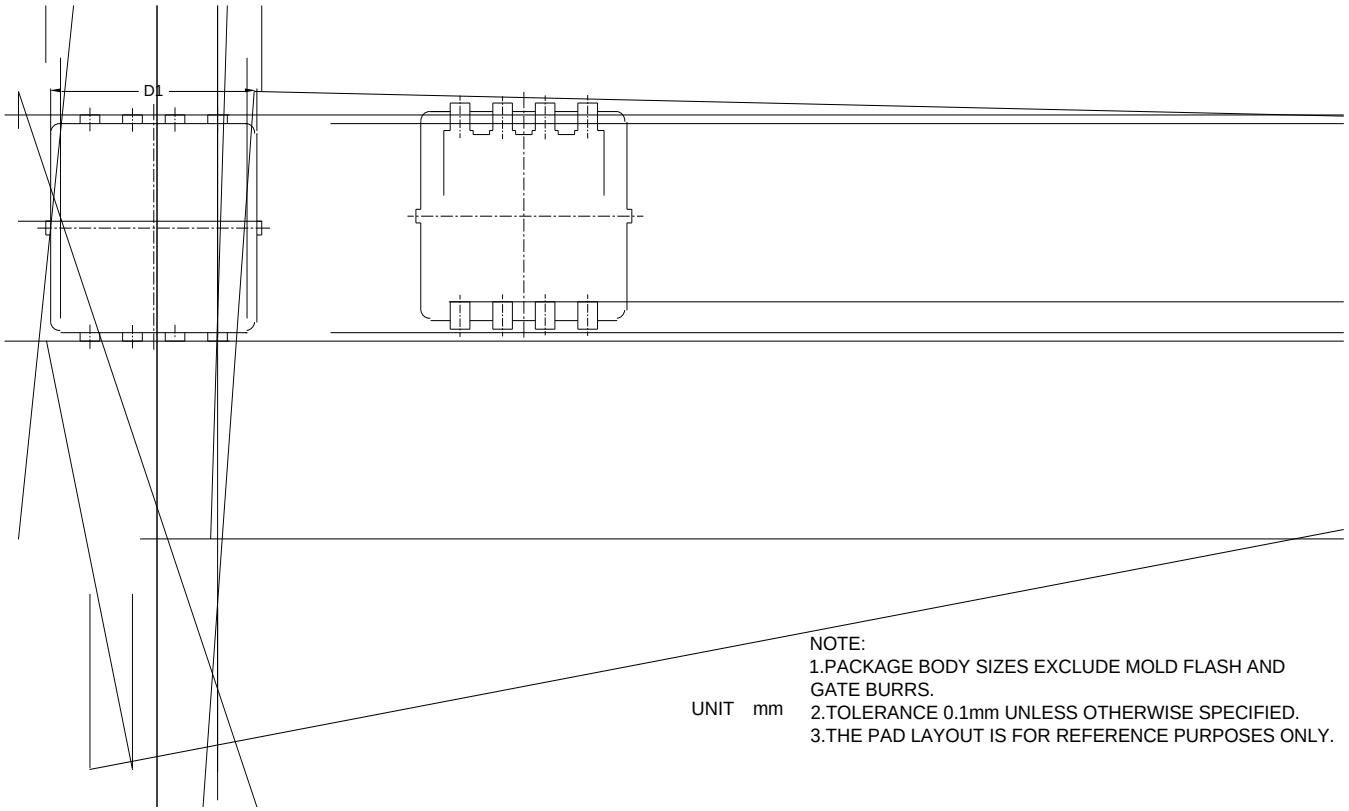


Figure D. Diode Recovery Test Circuit & Waveform

■ PDFN3333-8L-B Package information



UNIT mm

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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