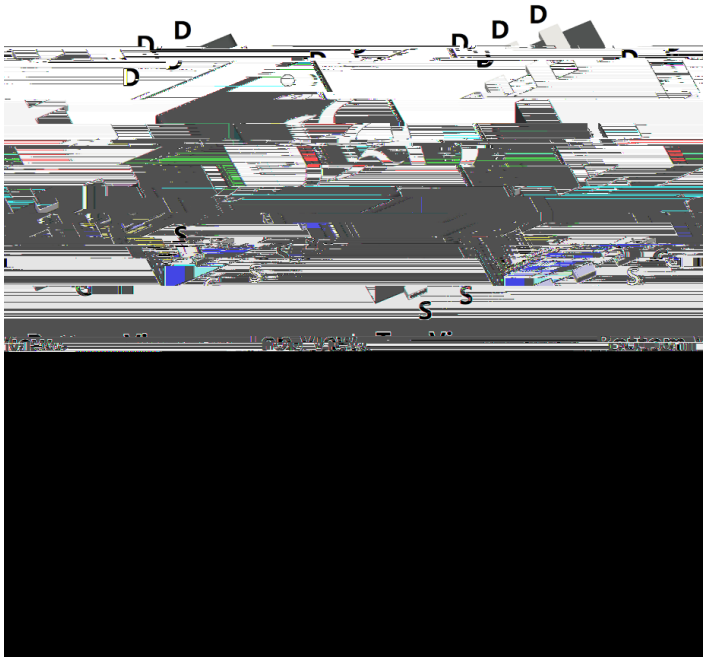
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 30V
- I_D 100A
- $R_{DS(ON)}$(at V_{GS}=10V) 2.1mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 4.5mΩ
- 100% EAS Tested
- 100% V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25	I_D	24	A
	T_A=100		15	
	T_C=25		100	
	T_C =100		63	
Pulsed Drain Current [A]		I_{DM}	400	A
Avalanche energy [B]		EAS	162	mJ
Total Power Dissipation [C]	T_A=25	P_D	2.5	W
	T_A=100		1	
	T_C=25		50	
	T_C =100		20	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	40	50	/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2	2.5	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ100G03AJR	F1	100G03A	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V	-	-	1	μA
		V_{DS}=30V, V_{GS}=0V, Tj=150	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=50A	-	1.6	2.1	mΩ
		V_{GS}=10V, I_D=20A		1.6	2.1	
		V_{GS}=4.5V, I_D=20A	-	2.5	4.5	
Diode Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	3	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	100	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=500KHz	-	2630	-	pF
Output Capacitance	C_{oss}		-	1830	-	
Reverse Transfer Capacitance	C_{rss}		-	100	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=15V, I_D=50A	-	45	-	nC
Gate-Source Charge	Q_{gs}		-	17	-	
Gate-Drain Charge	Q_{gd}		-	8	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A, di/dt=100A/us	-	40	-	n 1 32S

Typical Electrical and Thermal Characteristics Diagrams

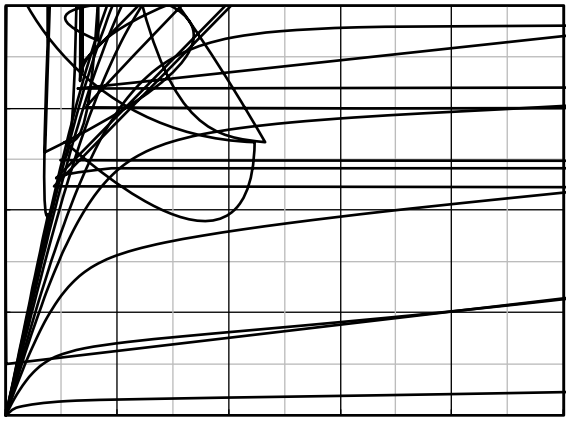


Figure 1. Output Characteristics

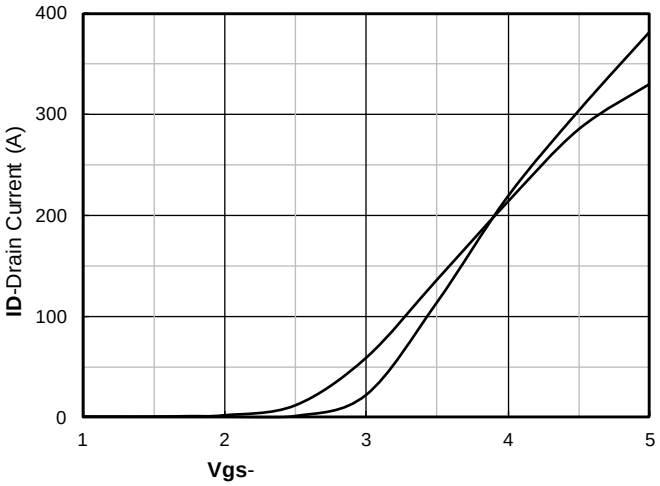


Figure 2. Transfer Characteristics

Figure 3. Capacitance Characteristics

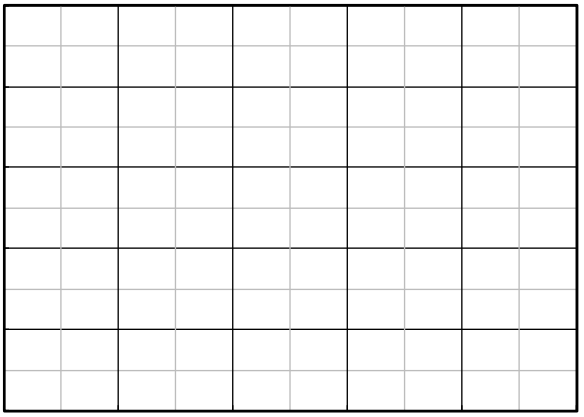


Figure 4. Gate Charge

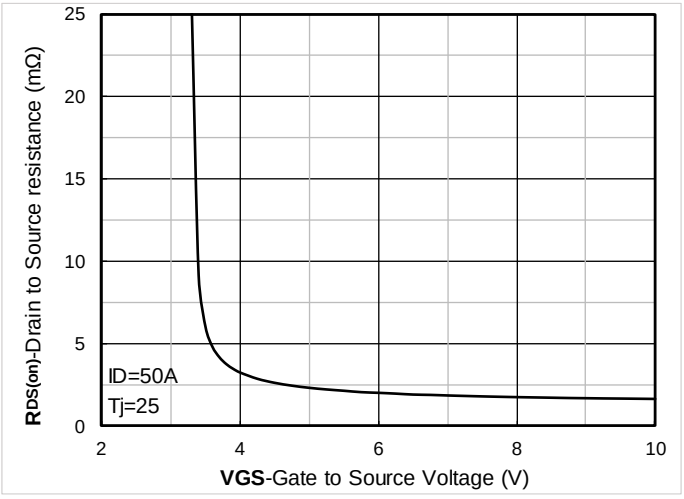


Figure 5. On-Resistance vs Gate to Source Voltage

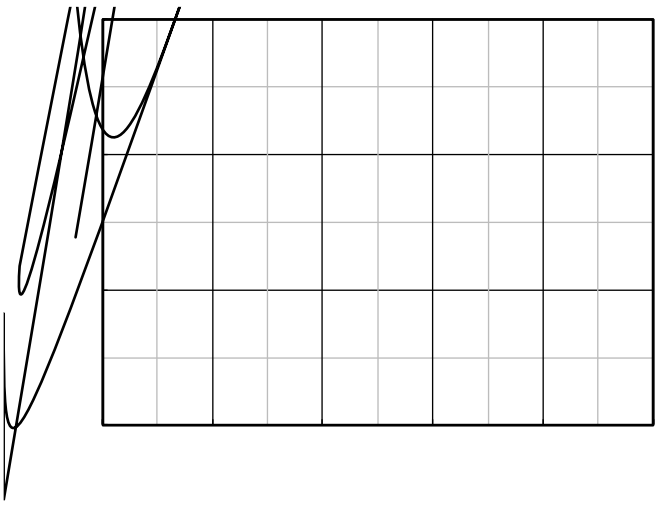


Figure 6. Normalized On-Resistance

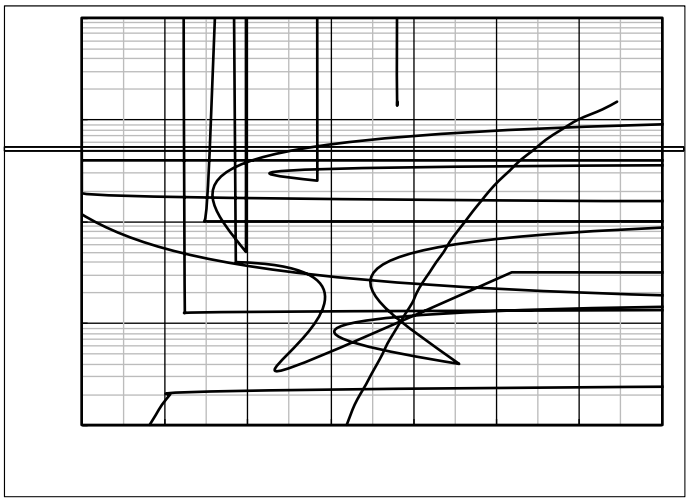


Figure 7. $R_{DS(on)}$ VS Drain Current

Figure 8. Forward characteristics of reverse diode

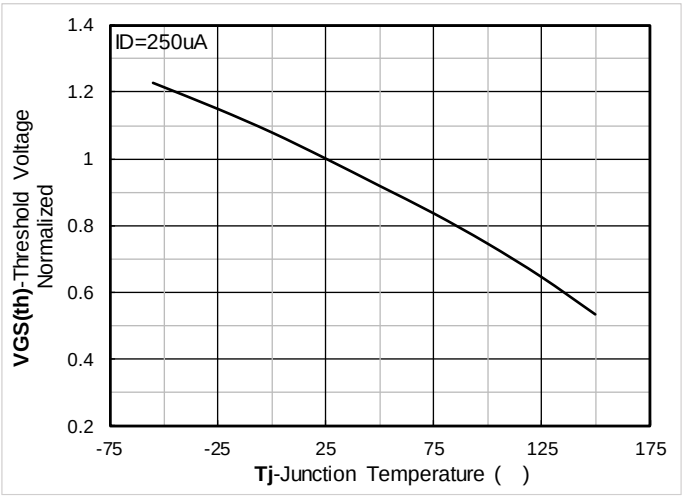


Figure 9. Normalized Threshold voltage

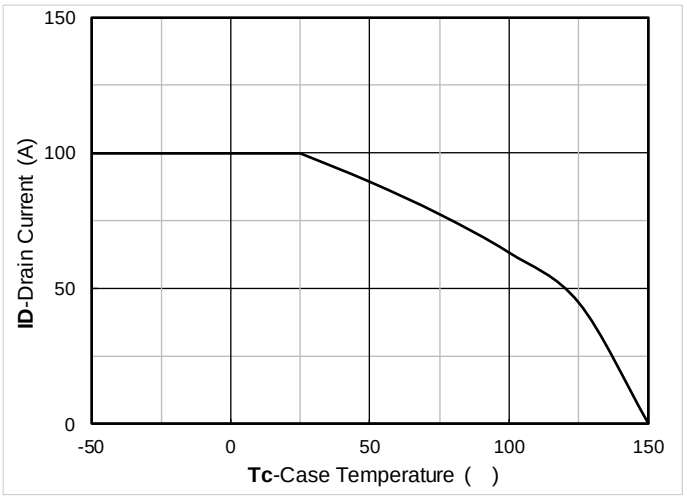


Figure 10. Current dissipation

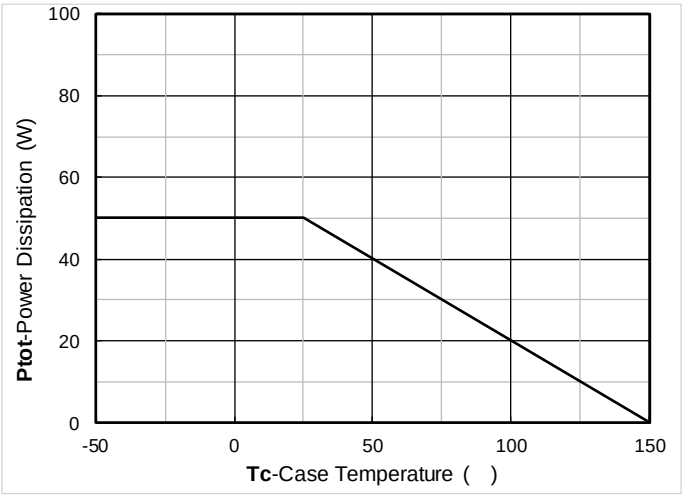


Figure 11. Power dissipation

Figure 12. Maximum Transient Thermal Impedance

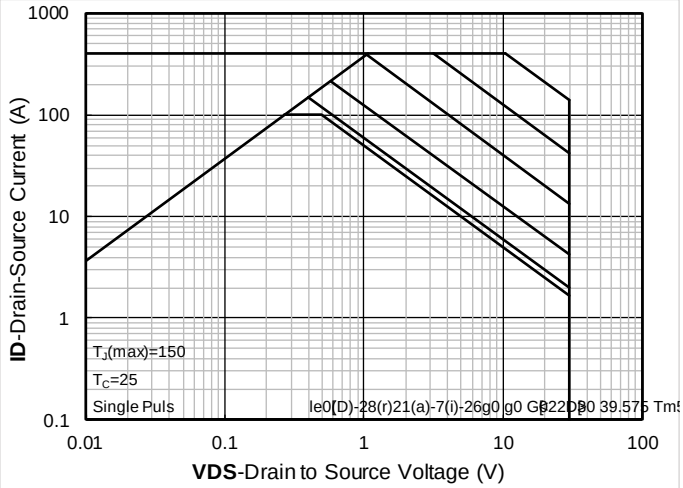


Figure 13. Safe Operation Area

■ Test Circ12P #MCID 7Lang (en-US)>BDC 0000000888 0 9Bit*nBT/F2108 Tf1 0 0 1 9 9 12Tm0 g0 G[Q1)2ETQ

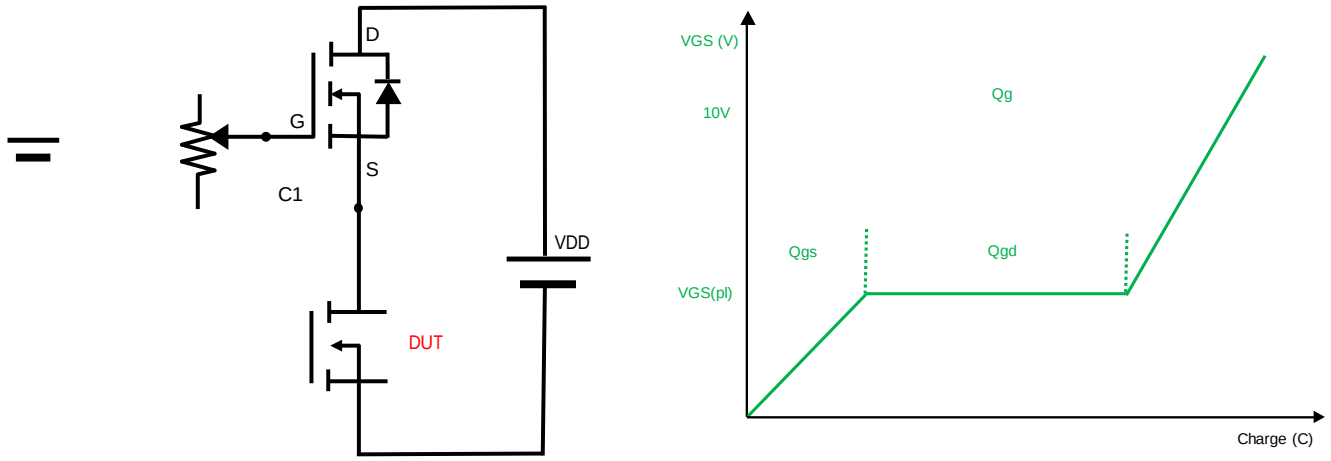


Figure B. Gate Charge Test Circuit & Waveform

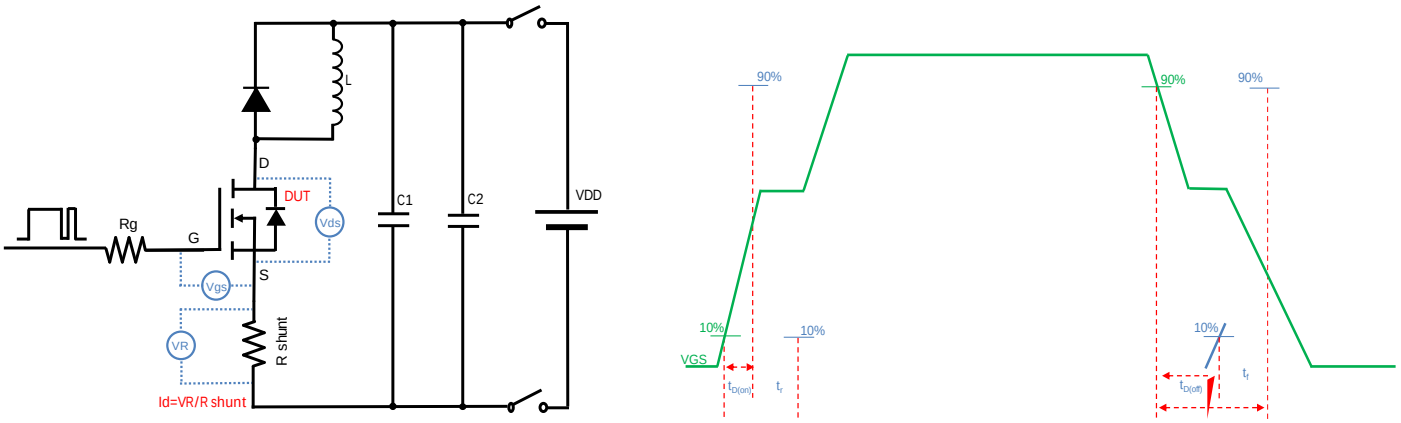


Figure C. Resistive Switching Test Circuit & Waveform

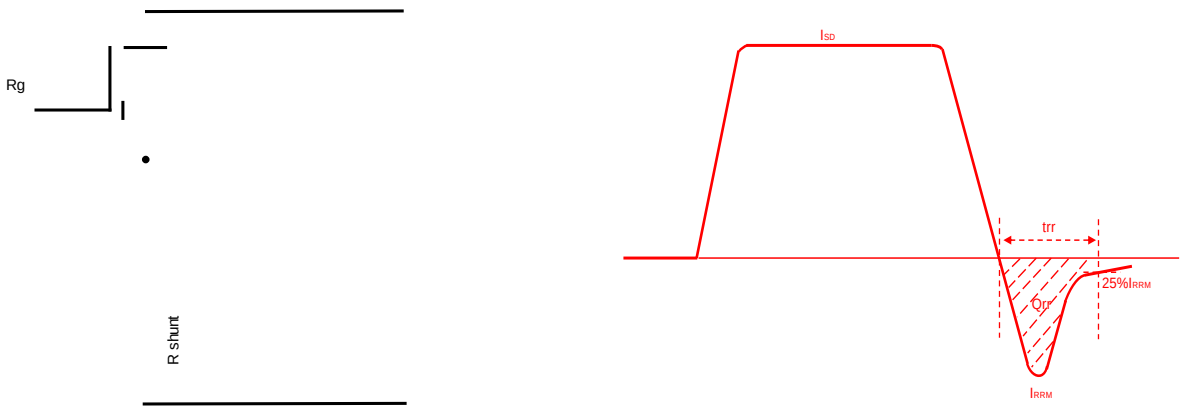
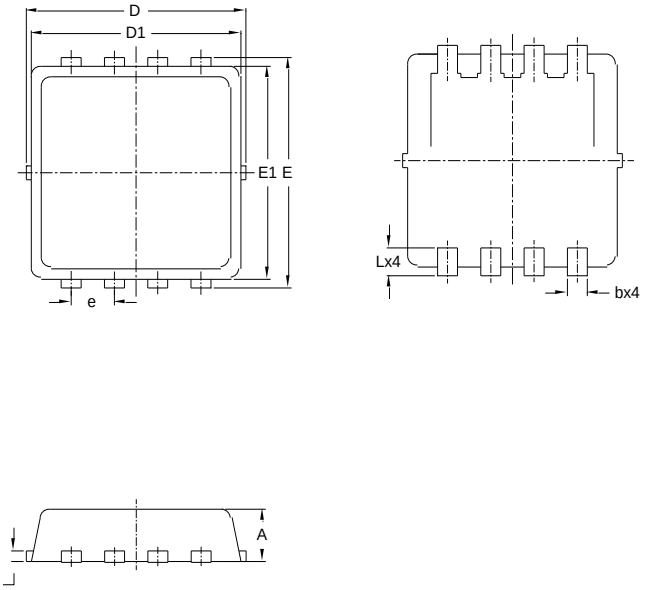


Figure D. Diode Recovery Test Circuit & Waveform

■ PDFN3333-8L Package information



UNIT mm

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.