



N-Channel and N-Channel Complementary MOSFET

Product Summary

- V_{DS} 40V
- I_D 30A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) 13m Ω
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) 20m Ω
- 100% EAS Tested
- 100% V_{DS} Tested

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply



YJGD30N04A

■ Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA



Typical Electrical and Thermal Characteristics Diagrams

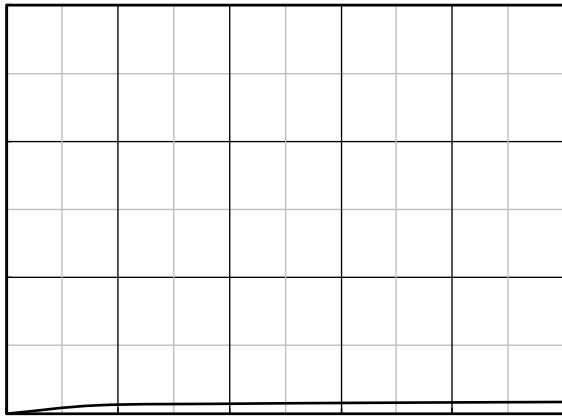


Figure 1. Output Characteristics

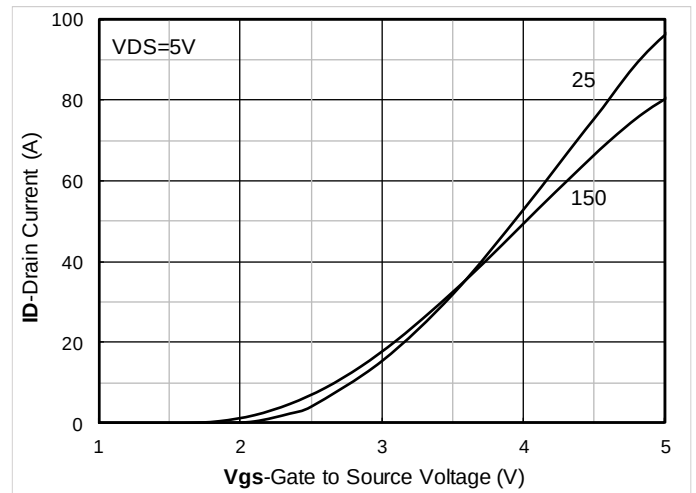


Figure 2. Transfer Characteristics

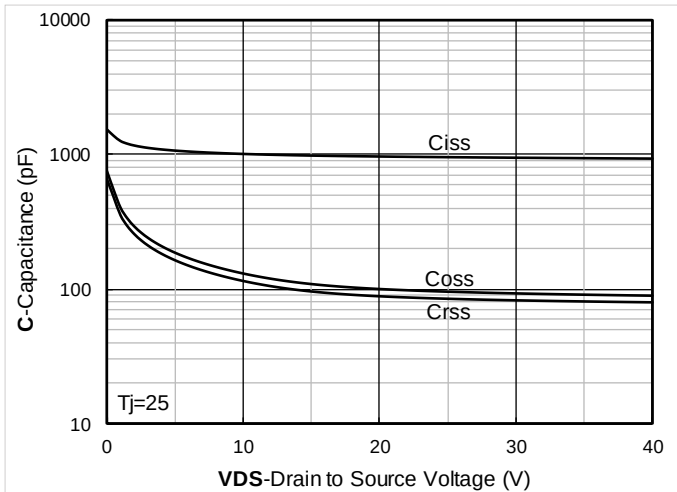


Figure 3. Capacitance Characteristics

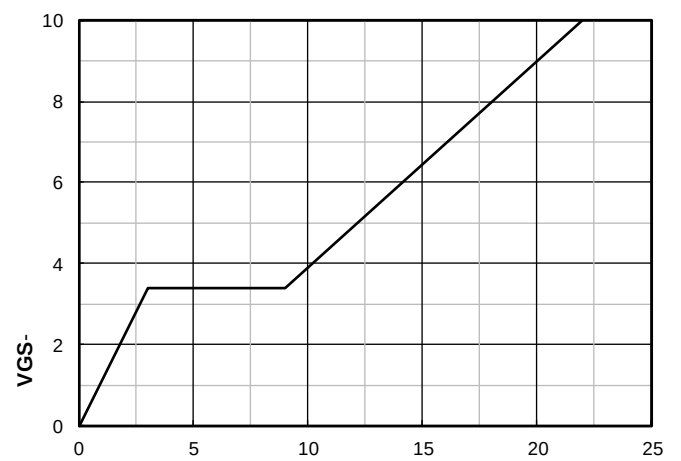


Figure 4. Gate Charge

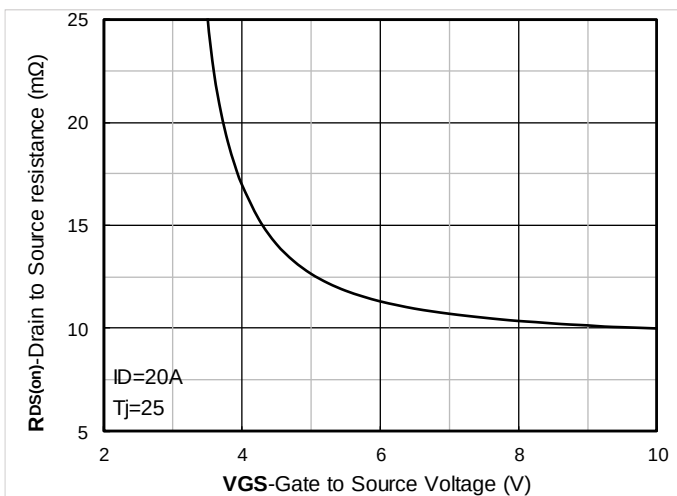
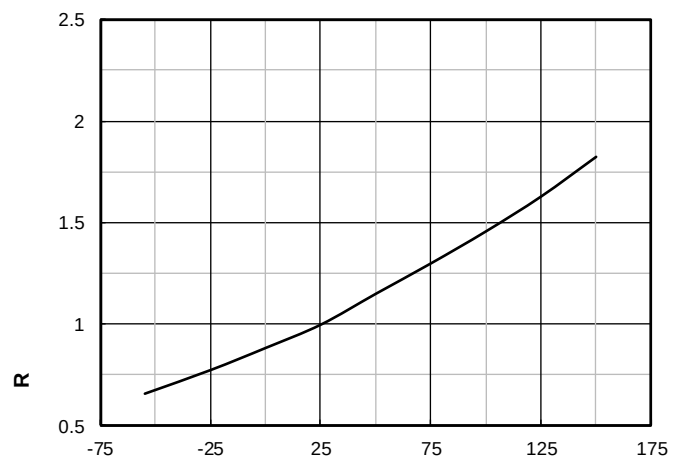


Figure 5. On-Resistance vs Gate to Source



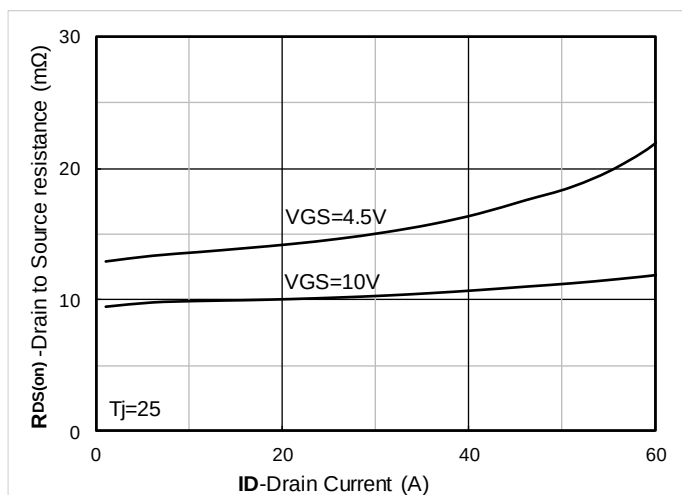


Figure 7.

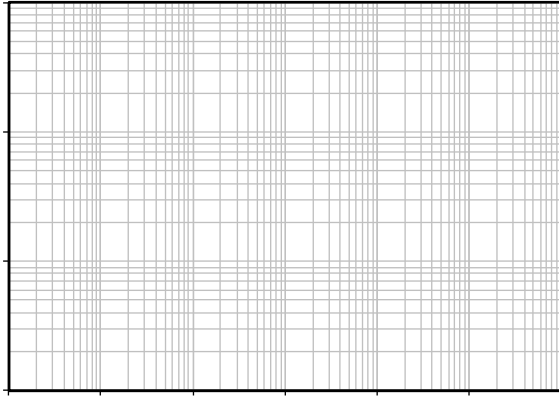


Figure 13. Maximum Transient Thermal Impedance

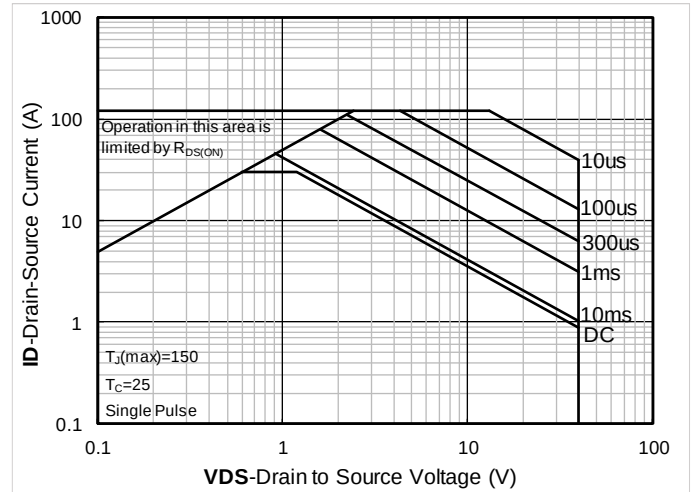


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

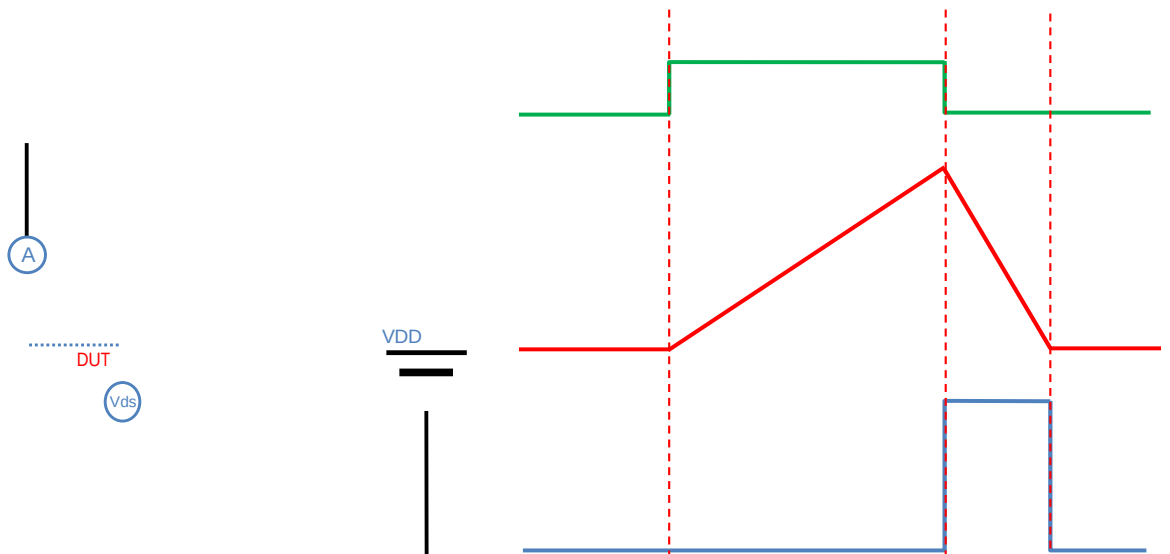


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

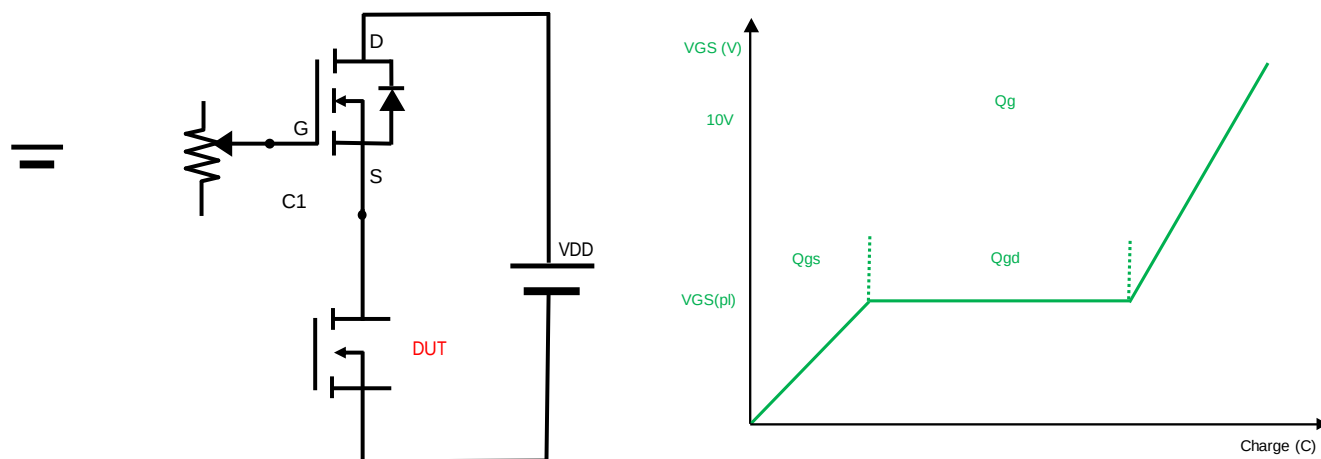
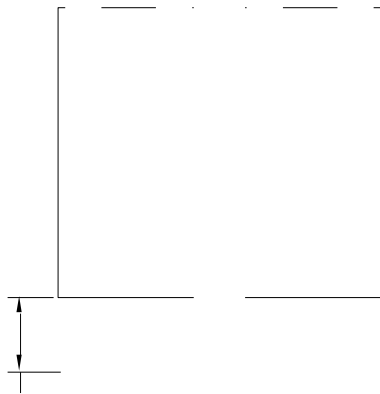


Figure B. Gate Charge Test Circuit & Waveform



■ PDFN5060-8L-E-1.1MM Package information



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.

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