NMOS(Die1/Die2)

● V_{DS}	60V
● I_D	20A
● $R_{DS(ON)}$(at V_{GS}=10V)	30mΩ
● $R_{DS(ON)}$(at V_{GS}=4.5V)	40mΩ
● 100% EAS Tested	
● 100% V_{DS} Tested	

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Part no. with suffix ”Q” means AEC-Q101 qualified

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- 12V, 24V Automotive systems

■ (T_A=25 unless otherwise noted)

Drain-so { ⸢ D				
Drain Current	T_A=25	I_D	6	A
	T_A =100		4	
	T_C=25		20	
	T_C =100		12.5	
Pulsed Drain Current [A]		I_{DM}	50	A
	T_C=25		69	
	T_C =100		27	
Thermal Resistance Junction-to-Ambient [D]		$R_{θJA}$	50	/W
Thermal Resistance Junction-to-Case		$R_{θJC}$	1.8	/W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	

■ (Example)

■ (T$_J$=25 unless otherwise noted)

Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		23	30	mΩ
		V_{GS}=4.5V, I_D=10A		28	40	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V			1.2	V
Gate resistance	R_G	f=1MHz		2		Ω
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1MHz		1250		pF
Output Capacitance	C_{oss}			80		
Reverse Transfer Capacitance	C_{rss}			60		
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
Gate-Source Charge	Q_{gs}	V_{GS}=10V, V_{DS}=30V, I_D=20A	-	3	-	nC
Gate-Drain Charge	Q_{gd}		-	6	-	
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=100A/us	-	17.5	-	nC
Reverse Recovery Time	t_{rr}		-	23.5	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=30V, I_D=20A Ry f				

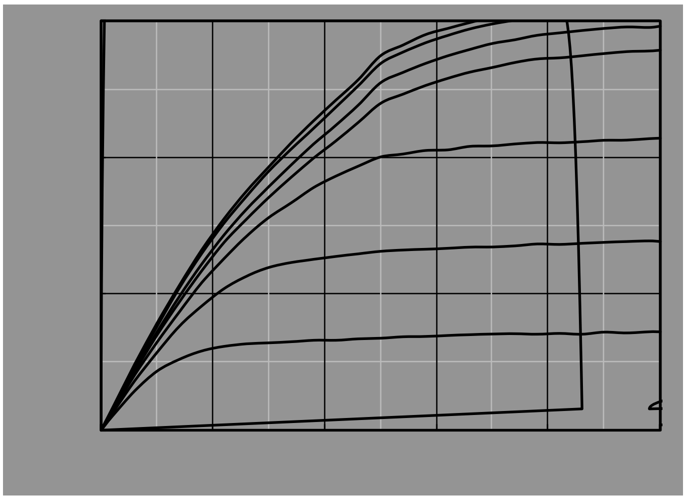

Figure 1. Output Characteristics

Figure 2. Transfer Characteristics

Figure 3. Capacitance Characteristics

Figure 4. Gate Charge

Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On-Resistance

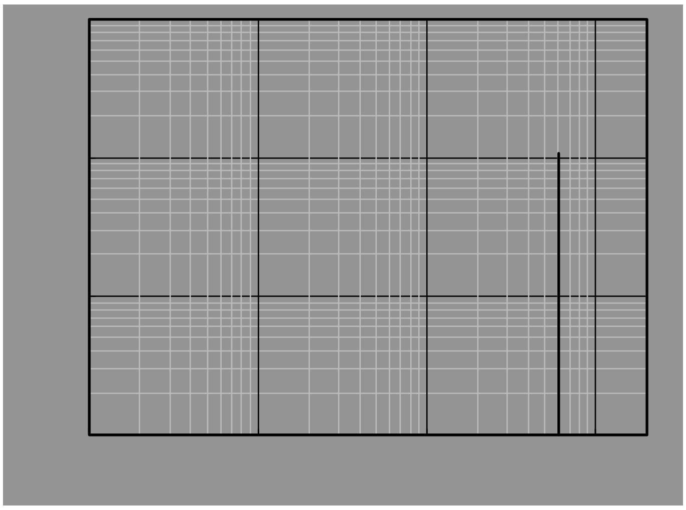

Figure 13. Maximum Transient Thermal Impedance

Figure 14. Safe Operation Area

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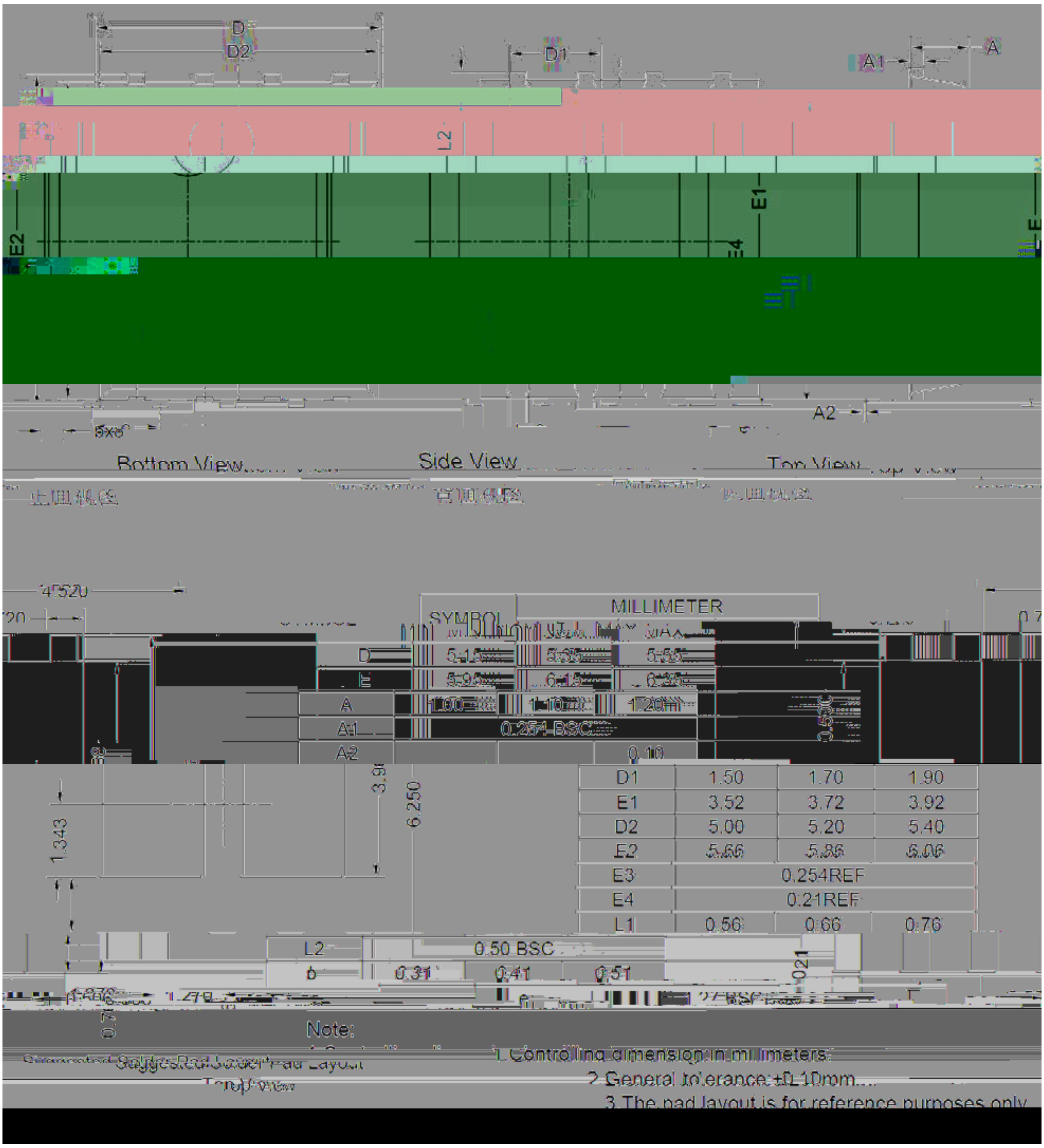

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	1.50	1.70	1.90
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254REF		
E4	0.21REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	27 BSC		

Note:

1. Controlling dimension in millimeters.
2. General tolerance ±0.10mm.
3. The pad layout is for reference purposes only.