N-Channel Enhancement Mode Field Effect Transistor

Product Summary

● V_{DS}	60V
● I_D	85A
● $R_{DS(ON)}$(at V_{GS}=10V)	5.2mΩ
● $R_{DS(ON)}$(at V_{GS}=4.5V)	8mΩ
● 100% EAS Tested	
● 100% V_{DS} Tested	

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter	Symbol	Limit	Unit

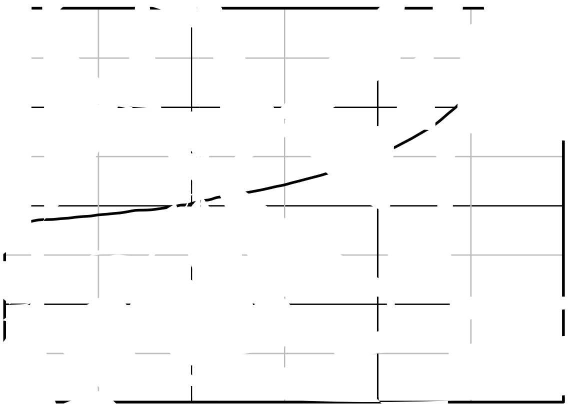

Figure 7. $R_{DS(on)}$ VS Drain Current

Figure 8. Forward characteristics of reverse diode

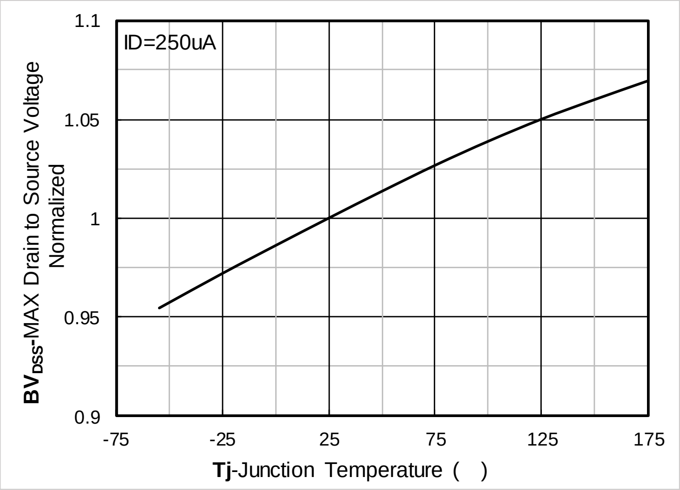

Figure 9. Normalized breakdown voltage

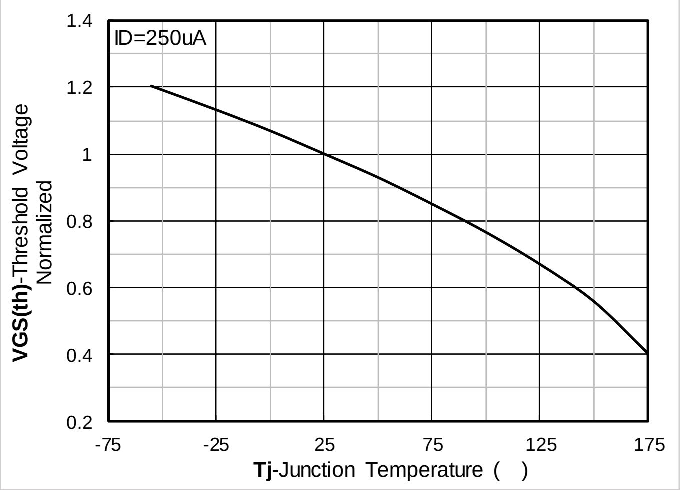

Figure 10. Normalized Threshold voltage

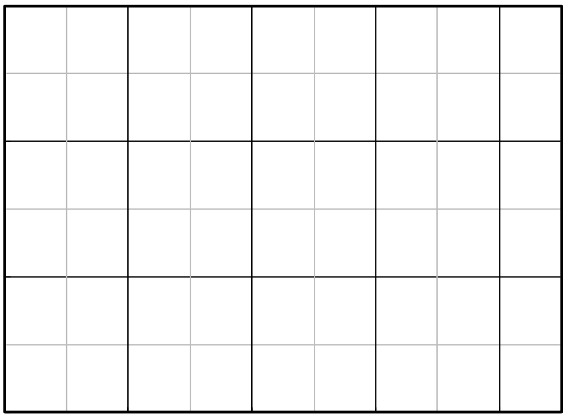

Figure 11. Current dissipation

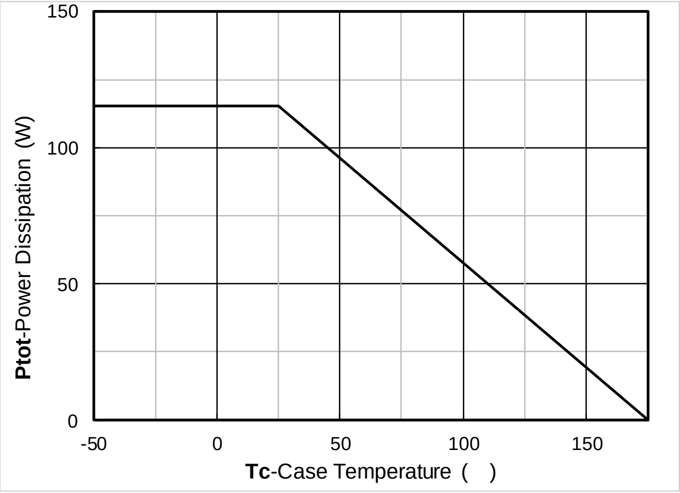

Figure 12. Power dissipation

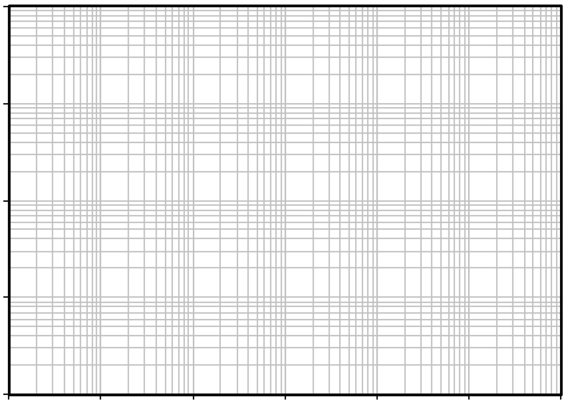

Figure 13. Maximum Transient Thermal Impedance

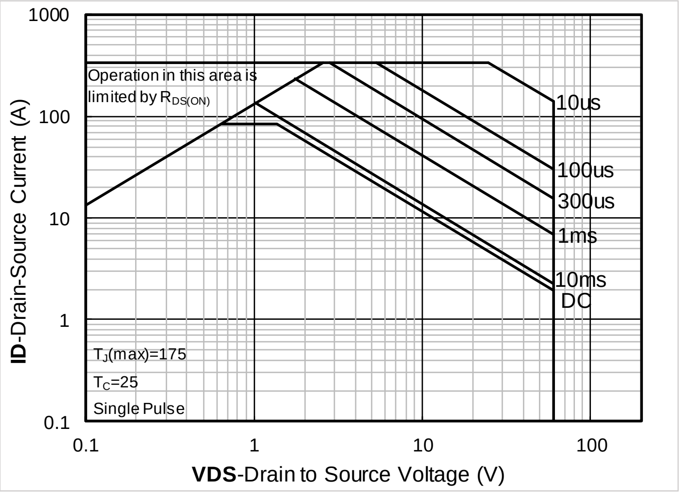

Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

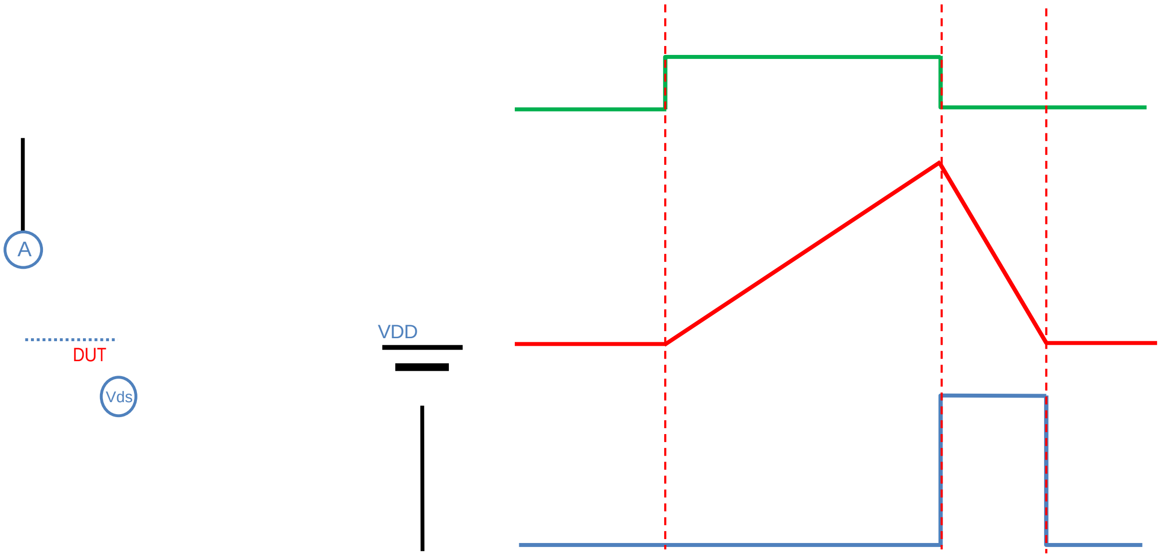

Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

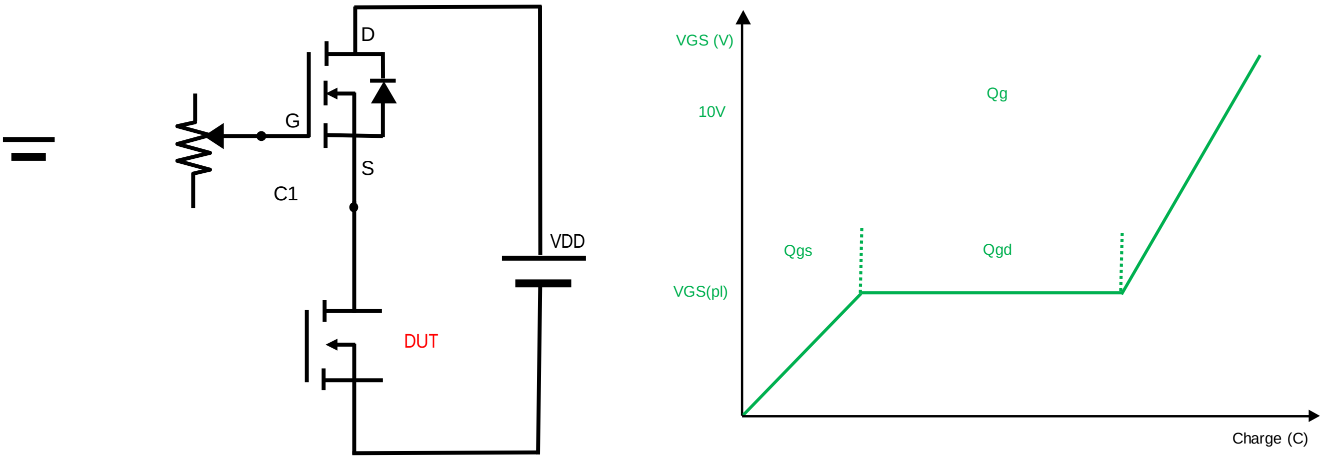

Figure B. Gate Charge Test Circuit & Waveform

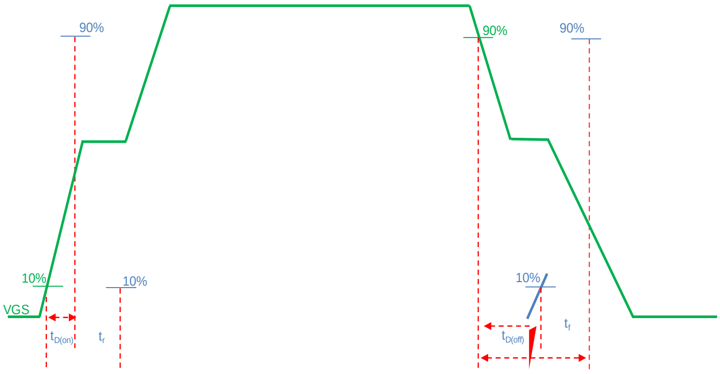

Figure C. Resistive Switching Test Circuit & Waveform

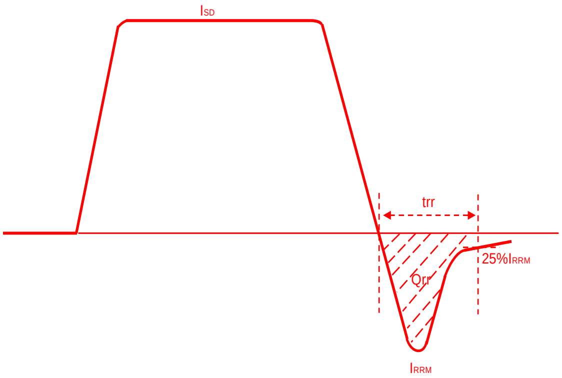

Figure D. Diode Recovery Test Circuit & Waveform

Dis/1.2rem0 g0.0000088bf3-8em0 mis/1.2re 59.84.2reW6 736 Tm