

# YJD30P04A

## P-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	-40 V
$I_D$	-30 A
$R_{DS(ON)}$ ( at $V_{GS}=-10V$ )	30 m
$R_{DS(ON)}$ ( at $V_{GS}=-4.5V$ )	45 m
100% EAS Tested	
100% $V_{DS}$ Tested	

### General Description

Trench Power LV MOSFET technology  
Low  $R_{DS(on)}$  & FOM  
Extremely low switching loss  
Excellent stability and uniformity  
High density cell design for low  $R_{DS(ON)}$   
Moisture Sensitivity Level 1  
Epoxy Meets UL 94 V-0 Flammability Rating  
Halogen Free

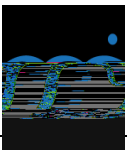
### Applications

### Absolute Maximum Ratings ( $T_A$ )

**YJD30P04A**

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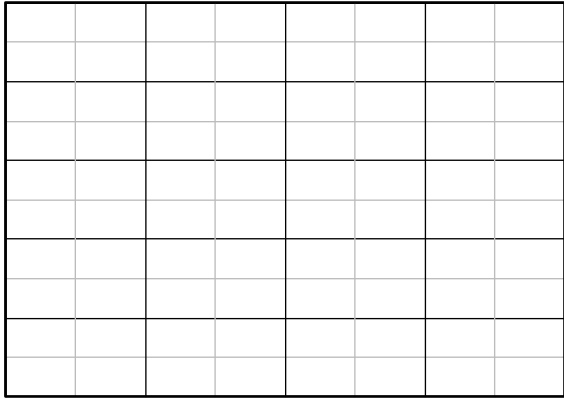


Figure 7.  $R_{DS(on)}$  VS Drain Current

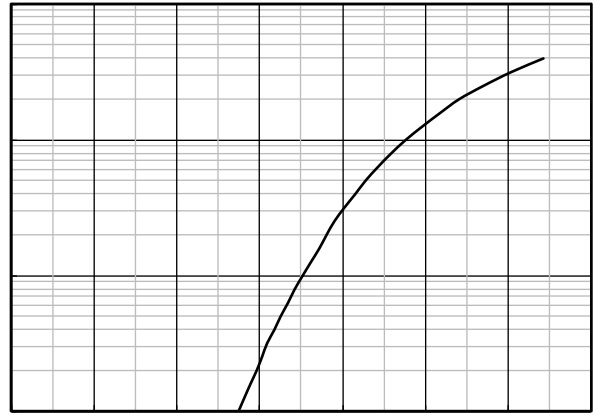


Figure 8. Forward characteristics of reverse diode

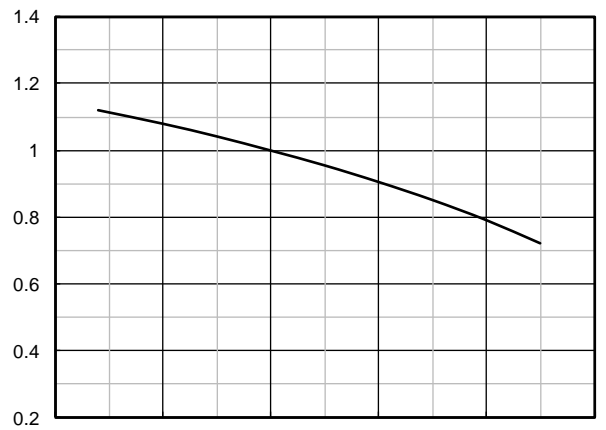


Figure 9. Normalized breakdown voltage

Figure 10. Normalized Threshold voltage

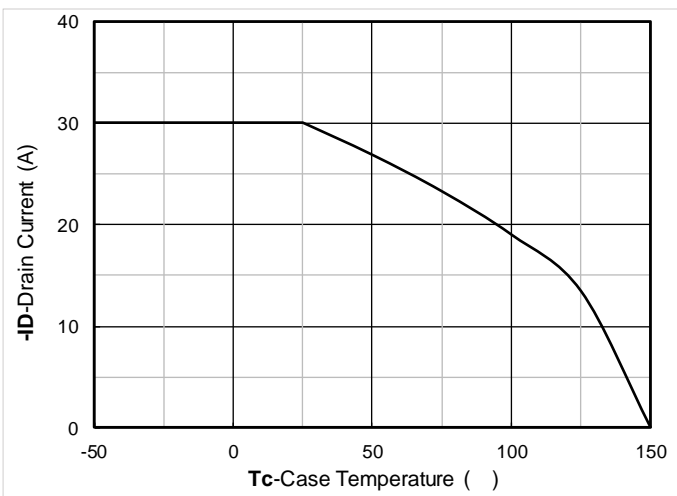


Figure 11. Current dissipation

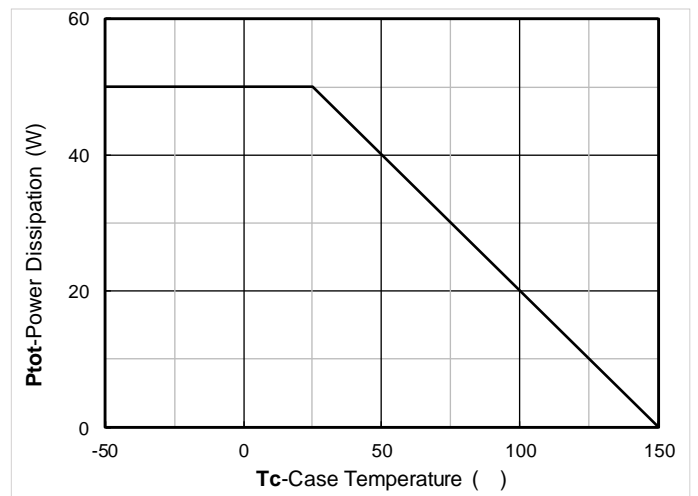
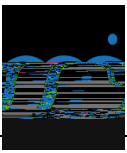
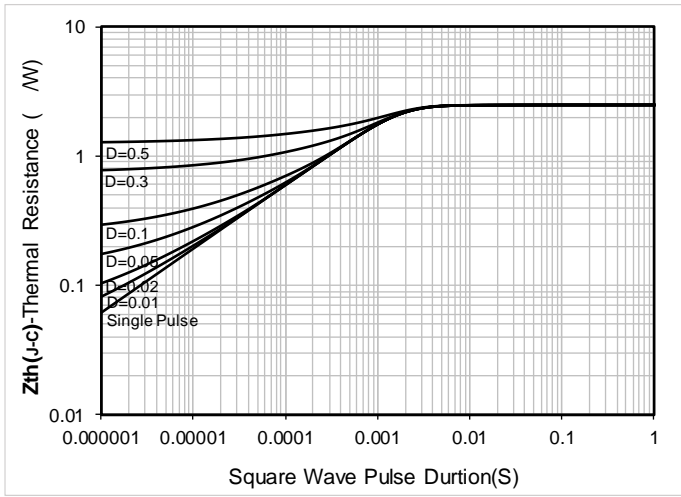
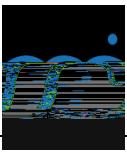


Figure 12. Power dissipation



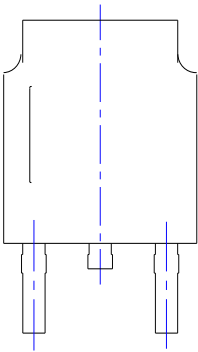
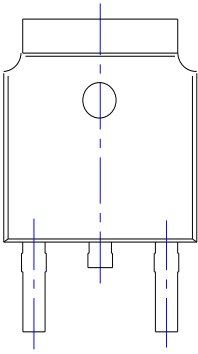
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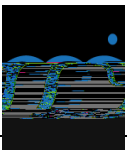
## TO-252-B Package information



SYMBOL	DIMENSIONS				
	INCHES				
	MIN.	NOM.			
A1	0.000				
A2	0.087	0.091			
A3	0.035	0.039			
b	0.026	0.030			
c	0.018	0.020			
D	0.256	0.260			
D1					
D2	0.181	0.189			
E	0.390	0.398			
E1	0.236	0.240			

**NOTE:**

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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## Disclaimer

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