N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	100V
I_D	12A
$R_{DS(ON)}$(at V_{GS}=10V)	120m
$R_{DS(ON)}$(at V_{GS}=4.5V)	135m

100% EAS Tested
100% V_{DS} Tested

General Description

Trench Power MV MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

Power management functions
DC-DC convertor

Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Volte		V_{DS}	100	V
Gat -source Volte		V_{GS}	±20	V
Drain Current	T_A=25	I_D	3	A
	T_A=100		2	
	T_C=25		12	
	T_C =100		8.5	
Pulsed Drain Current [A]		I_{DM}	25	A
Avalanche enersy [B]		EAS	12	mJ
Total Power Dissipation [C]	T_A=25	P_D	3	W
	T_A=100		1.5	
	T_C=25		50	
	T_C =100		25	
Junction d Stor491.se Temperature R491.nse		T_J ,T_{STG}	-55 +175	

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistnce Junction -to-Ambient [D]	Stdy -Stt	R	40	50	/W
Thermal Resistnce Junction -to-C491.se	Stdy -Stt	R	2.5	3	

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						

Drain

Typical Electrical and Thermal Characteristics Diagrams

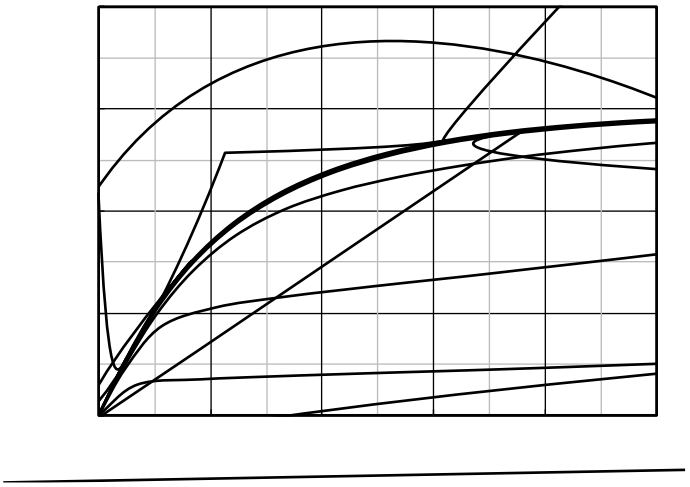


Figure 1. Output Characteristics

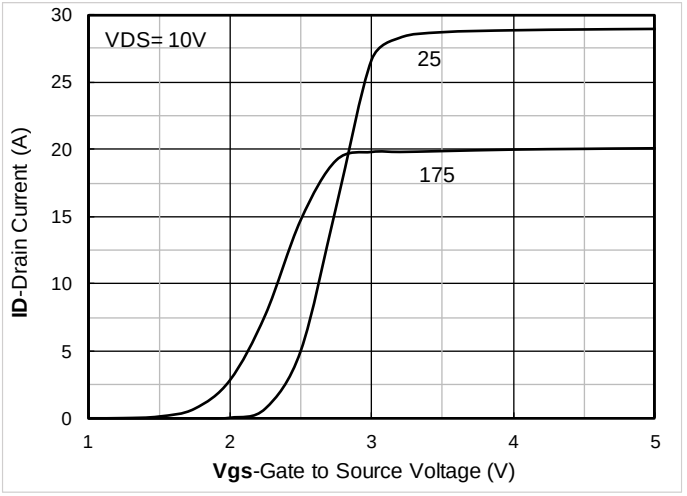


Figure 2. Transfer Characteristics

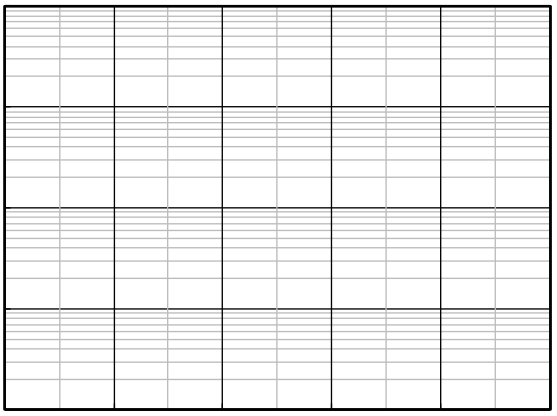


Figure 3. Capacitance Characteristics

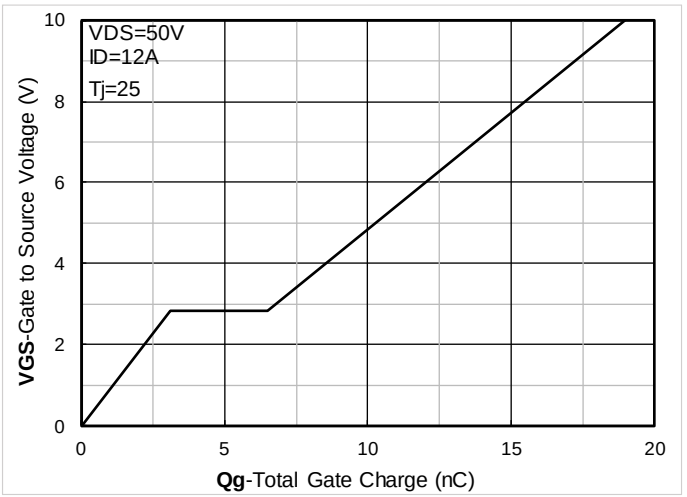


Figure 4. Gate Charge

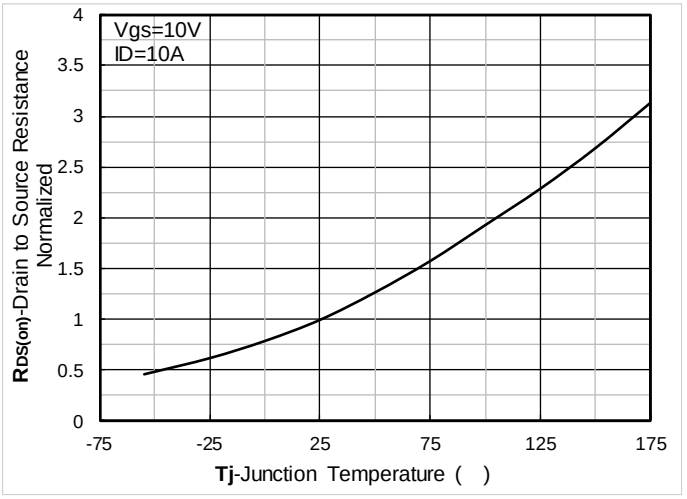


Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On-Resistance

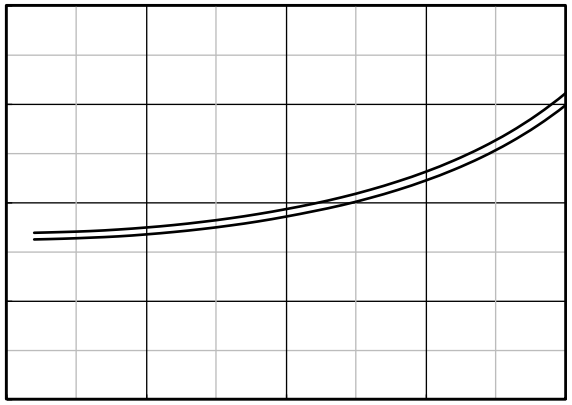


Figure 7. $R_{DS(on)}$ VS Drain Current

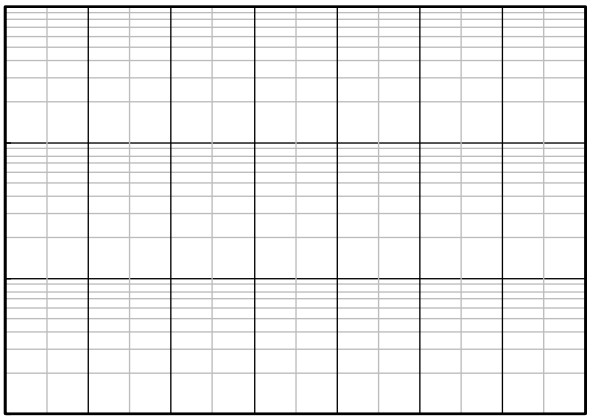


Figure 8. Forward characteristics of reverse diode

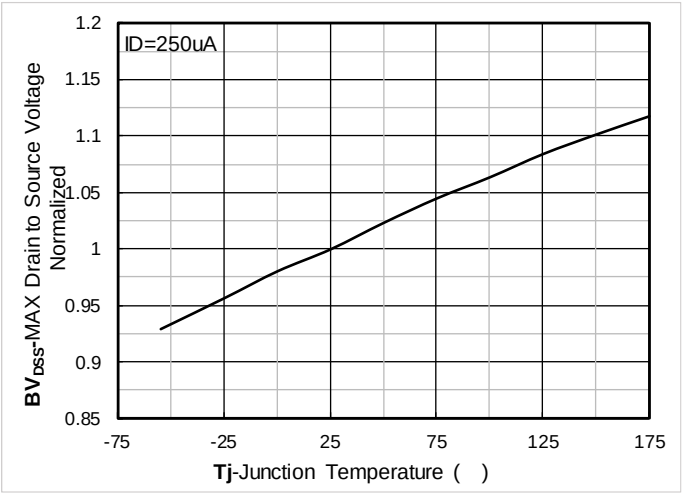


Figure 9. Normalized breakdown voltage

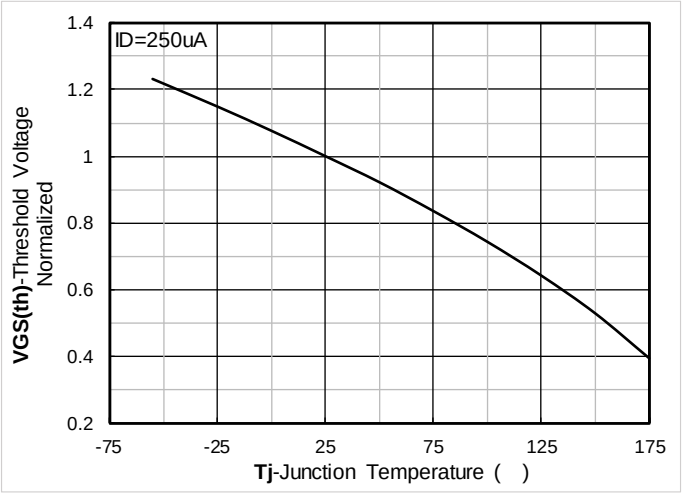


Figure 10. Normalized Threshold voltage

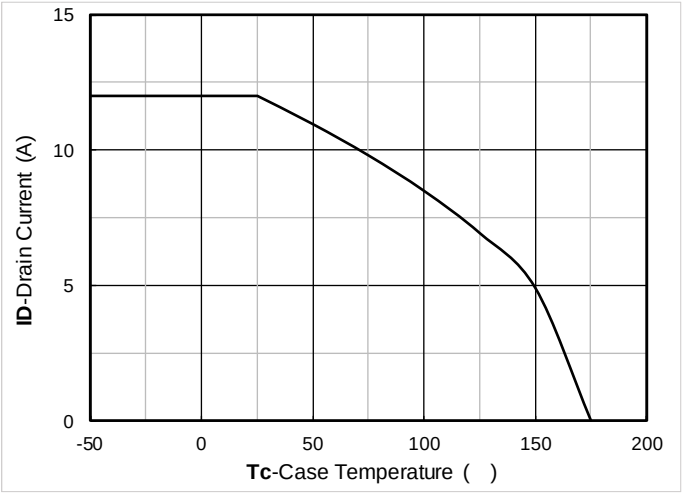


Figure 11. Current dissipation

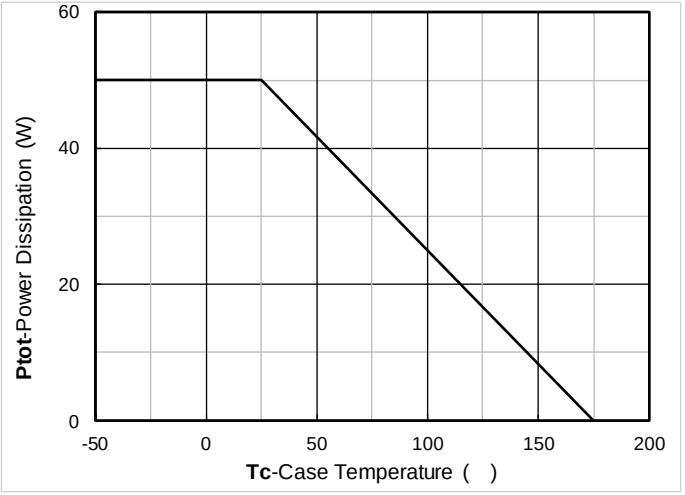


Figure 12. Power dissipation

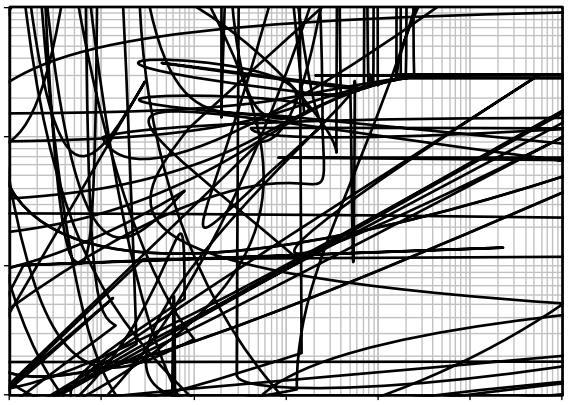


Figure 13. Maximum Transient Thermal Impedance

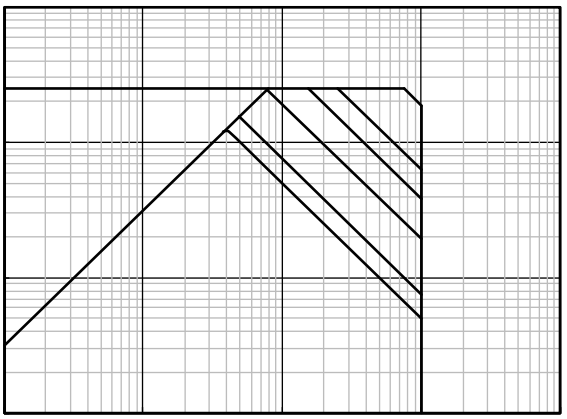


Figure 14. Safe Operation Area

Test Circuits & Waveforms

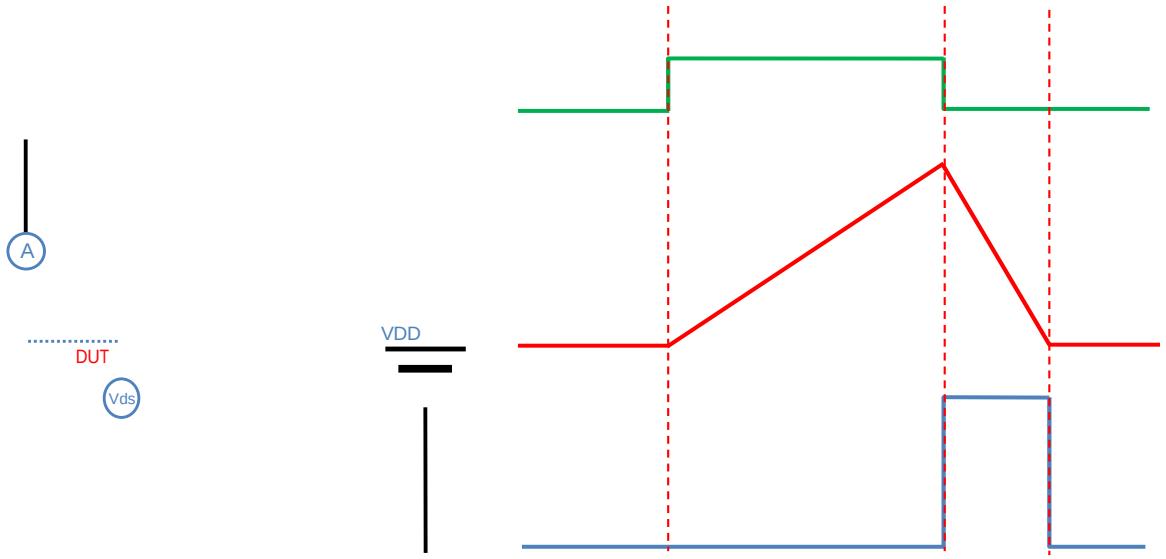
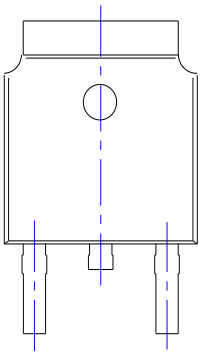
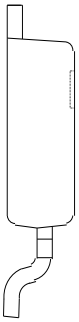


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

TO-252-B Package information

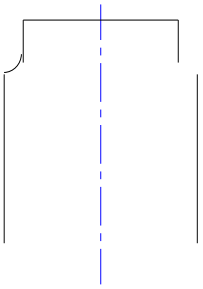


TOP VIEW



SIDE VIEW

DIMENSIONS					
SYMBOL	INCHES				
	MIN.	NOM.			
A1	0.000				
A2	0.087	0.091			
A3	0.035	0.039			
b	0.026	0.030			
c	0.018	0.020			
D	0.256	0.260			
D1					
D2	0.181	0.189			
E	0.390	0.398			
E1	0.236	0.240			



BOTTOM VIEW

SUGGESTED SOLDER PAD LAYOUT

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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